CIS2521AF

5.5 Megapixel CMOS Image Sensor

Datasheet

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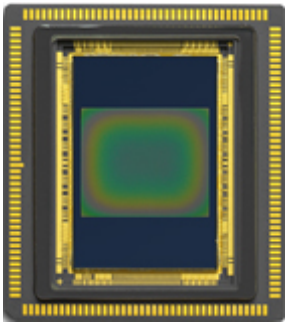
PRODUCT DESCRIPTION (Rev: K)

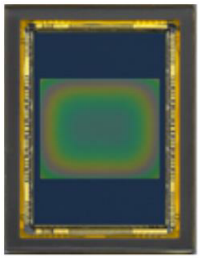
The CIS2521AF offers outstanding features and performance for scientific, industrial, and medical applications.

FEATURES

- **5.5 Megapixel (2560 Horizontal x 2160 Vertical) CMOS Image Sensor**
- **4/3" optical format**
- **Ideal pixel size for scientific applications**
  - **6.5 µm x 6.5 µm pixel area, 5T pixel**
- **High frame rates at full resolution**
  - **100 fps in Rolling Shutter readout mode**
  - **50 fps in Global Shutter readout mode**
- **Enables ultra-low-light imaging**
  - **< 2.0 e- noise**
- **Flexible windowing to allow faster frame rates**
  - **Programmable ROI readout**
- **Low dark current so deep cooling not needed**
  - **< 35 e-/pixel/second dark current @ 20°C**
- **High sensitivity visible through NIR**
  - **≥ 55% peak quantum efficiency (QE)**
- **Record intense & faint features simultaneously**
  - **> 83.5 dB intra-scene Dynamic Range (WDR) mode**
- **Digital sensor for more compact designs**
  - **On-chip column parallel 11-bit A/D converters**
  - **Dual gain 11-bit output channels per pixel**



CIS2521AF0121
FX1(CLCC168 pin) Scientific Package



CIS2521AF0221
FX2 (CLCC168 pin) standard Package

The CIS2521AF is a large format, ultra-low noise CMOS image sensor intended for applications requiring high quality imaging under extremely low light conditions. The device features an array of 5 transistor (5T) pixels on a 6.5µm pitch with an active imaging area of 2560(H) x 2160(V) pixels. The CIS2521AF delivers extreme low-light sensitivity with read noise less than 2 electrons RMS, Quantum Efficiency (QE) above 55% and very low dark current. The sensor runs in Rolling and Global Shutter readout modes. The sensor has two ADC channels per column with one optimized for low light levels and the other optimized for high light levels, enabling high dynamic range data collection in a single image. The sensor supports user-programmable row start/stop control for region of interest (ROI) readout. The sensor is housed in a 168-pin CLCC package (Scientific and Standard packages are shown above). These features, combined with 5.5 megapixel resolution and 100 fps imaging rates, make the CIS2521AF an imaging device ideally suited for a variety of low light-level camera applications including: security/surveillance, industrial, and medical.

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1 Features and General Specifications

1.1 Electro-optical Specifications

Table 1 contains the electrical-optical parameters and specifications for the CIS2521AF image sensor.

Table 1: Electro-optical specifications

Parameter	Specification	Notes
Intra-frame dynamic range	15000:1	
PRNU	< 3% RMS	Measured at 1x LG
Dark current	< 35 e-/pixel/sec	at 20ºC
Dark Signal Non Uniformity (DSNU)	< 2% RMS	Measured at 1x LG
Conversion gain (DN/e-)	High gain output (nominal): − 1.7 at 30x − 0.57 at 10x Low gain output (nominal): − 0.12 at 2x − 0.06 at 1x	ADC input range is programmable from 0.4V to 1.55V. Therefore, conversion gain in DN/e- is programmable.
Full well capacity (FWC)	≥ 30,000 e-	
Lag	< 3 e-	
Non-linearity	< 2%	
Fill factor with microlens	> 0.9	
Microlens F#	1.5 for monochromatic sensor 1.6 for color sensor	
Peak QE	≥ 0.55	at 600nm
Temporal read noise	< 2 e- RMS @ 30 fps Rolling Shutter readout	Median value of read noise distribution from high gain output (30x gain)

The above specifications are from CIS2521AF devices running in Rolling Shutter mode. Although the CIS2521AF runs in Global Shutter mode, BAE does not guarantee any performance specifications for Global Shutter mode.

For sensor performance specifications in photometric units, contact Technical Support at cams.techsupport@baesystems.com.

1.2 General Specifications

Table 2 contains typical values of general parameters for the CIS2521AF image sensor.

Table 2: Parameters and Typical Values

Parameter	Typical value
Active array size	2560 (H) x 2160 (V), imaging pixels only 2592 (H) x 2192 (V), imaging and dark pixels
Pixel size	6.5 µm x 6.5 µm
Dimensions of active area (Note 1)	16639.6 µm (H) x 14039.6 µm (V), imaging pixels only 16847.6 µm (H) x 14247.6 µm (V), imaging and dark pixels
Dimensions of die (Note 2)	18842 µm (H) x 27642 µm (V), die circuit only 18882 µm (H) x 27682 µm (V), including seal ring 19002 µm (H) x 28122 µm (V), including saw street (estimate)
Shutter type	Rolling Shutter, Global Shutter (snapshot). ROI readout capabilities for both shutter types.
Maximum frame rate (Note 3)	100 fps (Rolling Shutter) 50 fps (Global Shutter)
Number of readout ports	2 (1 for top half array, 1 for bottom half array)
Maximum line rate (Note 3)	109.6 kHz (9.124 µs/line)
Maximum pixel rate (Note 3)	284 MHz (3.48 ns/pixel)
ADC resolution	2 x 11-bit
Column level amplifier gain	1x or 2x (low gain output) 10x or 30x (high gain output)
Power consumption	< 2 W
I/O interface	1.8V LVCMOS and 1.8V HSTL (class I)
Package type	168-pin LCC
Optical format	4/3 ”

Note 1: Dimensions are from the lithographic pattern.

Note 2: The dimensions for the die circuit area and the seal ring around it are defined by lithography and are accurate to sub-micron tolerances. When the die is cut from the wafer, there may be greater variations depending on the wafer cut process.

Note 3: The values for line rate and pixel rate are calculated values based on the assumption of 100 fps operation. If the sensor is running 100 fps, one frame takes 0.01 seconds and there are 1096 lines in a frame (for each sensor half, assuming the default frame size). Therefore each sensor half has a maximum line rate of 109.6 kHz. Each line has 2592 pixels, so the maximum pixel rate is (2592 pixels/line)*(1096 lines/frame)*(100 frames/sec) = 284,083,200 pixels/second, or 284 MHz.

Because these values for maximum pixel and line rates are calculated values, what the numbers are actually showing is maximum average line rate and maximum average pixel rate. On chip, the maximum SCLK input is 287 MHz, and the digital numbers for each pixel value come out at a rate of one per SCLK (for each imager half). So actual pixel data may be appearing on the DOUT and DOUT_LG pins at the SCLK rate of 287 MHz, at least for the portion of each line time that pixel readout is occurring (2592 SCLKs out of every 2624 SCLKs).

If the 100 fps number is not assumed but is instead calculated from on-chip functionality, a slightly different fps number can be found. In the CIS2521AF sensor, the number of clocks per row of pixels is set by JTAG Registers 16 through 47, which together are called the “wavetable”. According to both default and recommended wavetable settings, there are 2624 SCLK clocks per line. This then correlates to a line time of (2624 clocks/line) / (287 million clocks/sec) = 9.142 µs/line. The maximum frame rate then depends on the number of lines in the frame. The number of lines in the frame is controlled by the user loading values into JTAG Registers 6, 7, and 8. With the default values that are automatically loaded at device start up, the frame is 1080 imager lines plus 16 dark lines = 1096 lines. Therefore, the Rolling Shutter maximum frame rate with default settings is:

(287 million clocks/sec) / (2624 clocks/line)*(1096 lines/frame) = 99.79 frames/second

Which is rounded up to 100 fps in Table 2. (Obviously much higher frame rates are possible if smaller frame sizes are used in place of the default 1096 lines.) Note that the actual image with the default settings will actually be 1096*2 = 2192 rows high, since the “1080” and “16” numbers are with respect to the imager half, and the final image consists of both top and bottom halves.

The maximum frame rate for Global Shutter is always ½ the maximum frame rate for Rolling Shutter (assuming equal frame sizes and SCLK frequencies), since two frames of sensor readout (the Reset frame and the Data frame) are necessary to construct the final Global Shutter image.

2 Functional Description

2.1 Architectural Overview

2.1.1 Block Diagram

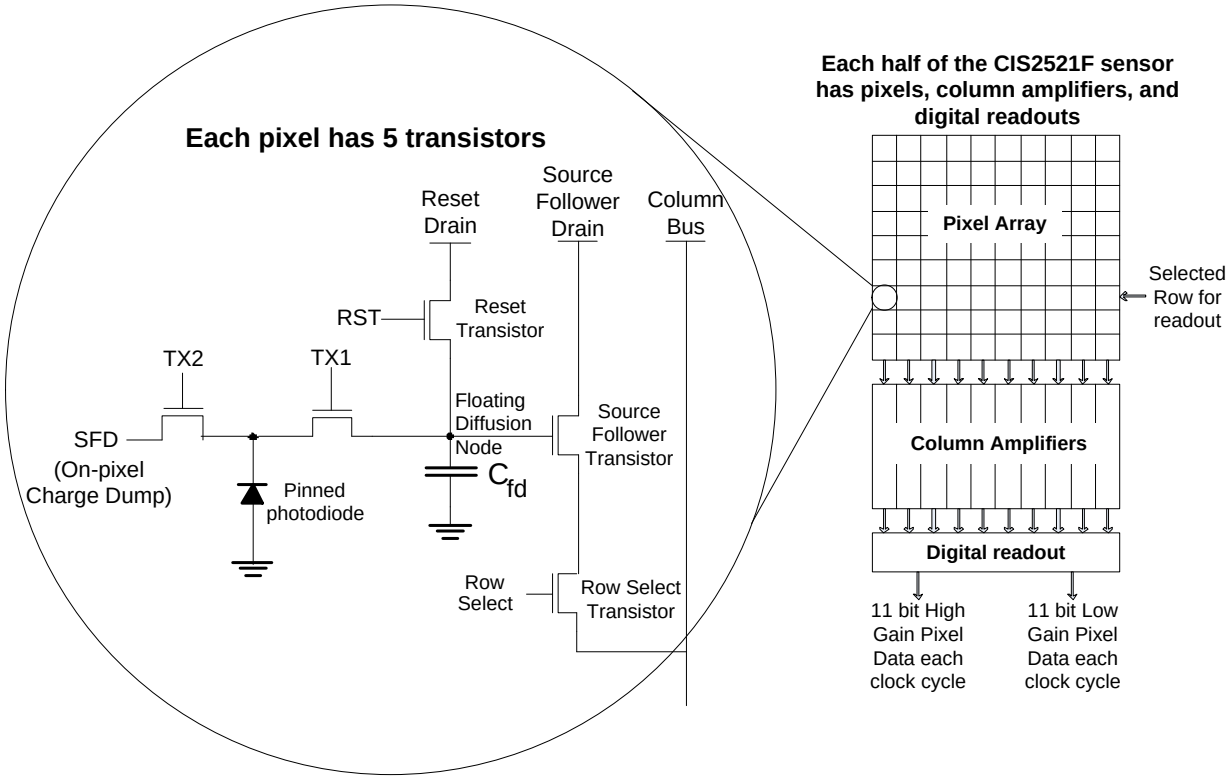


Figure 1. Block Diagram of CIS2521AF

The sensor is run as two independent halves. Figure 1 shows a simplified block diagram for one sensor half. The two halves are symmetric.

Each half has:

1) Pixels to collect photo-charge and convert the magnitude of that photo-charge to an analog voltage
2) Column amplifiers to amplify and then digitize the incoming analog voltages from the pixels
3) Digital readout circuitry to read out the digital numbers created by the ADCs in the Column Amplifiers to the data output pins of the sensor

   (DOUT[10:0] for High Gain data, and DOUT_LG[10:0] for Low Gain data)

2.1.2 Sensor Floor Plan

The sensor consists of two independent halves. The pixel orientation is identical in both halves. The column amplifier circuits, ADCs and the Digital control block (DCB) are located at the top and bottom of the array. The row control circuits are located on both sides of the pixel array.

Note the symmetric character of this layout. The top half will be read out according to the Register settings in the Digital control block of the top half. The bottom half will be read out according to the Register settings in the Digital control block of the bottom half. Typically, the Register settings will be identical between the top and bottom halves, though this is not always the case (e.g. see “Pseudo Single Port” operation, described in “MAN 0102”, the CIS2521AF Programming Manual).

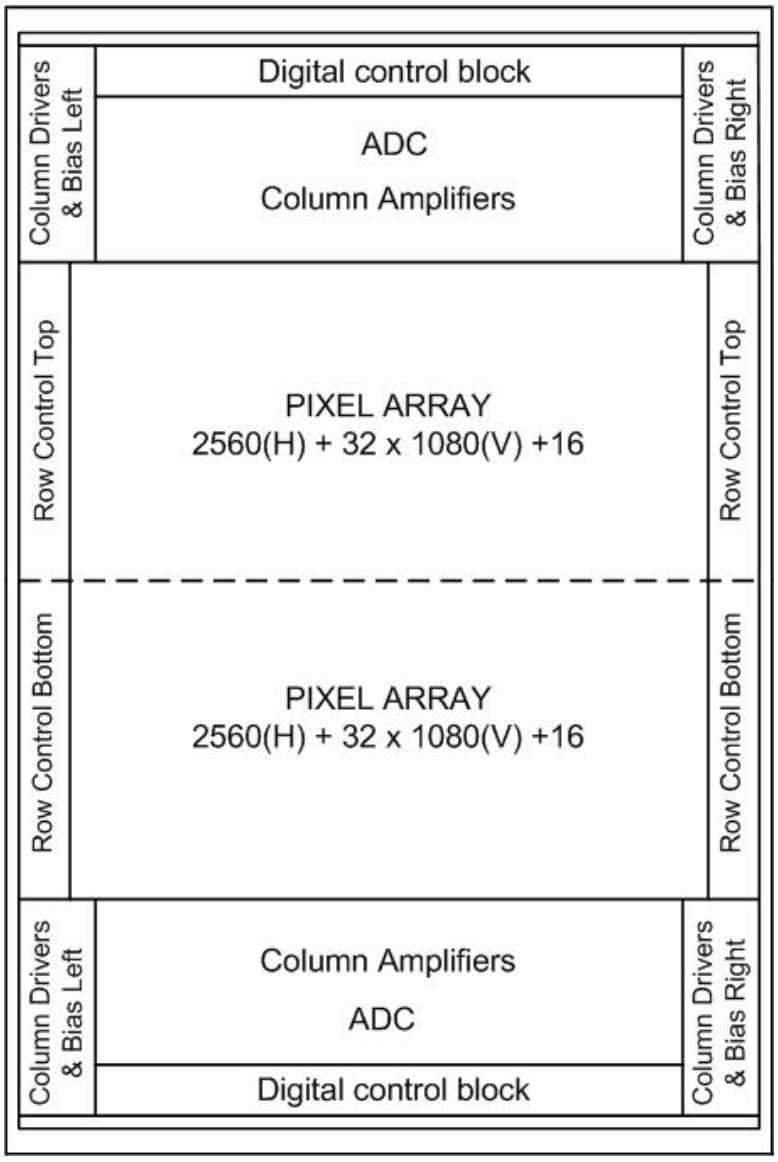


Figure 2. Sensor floor plan

The 2560 by 2160 active imager pixel array is surrounded on all sides by a 16 pixel wide dark region. Rows are numbered with row 0 in the center and with numbers increasing moving outward from the center. Because the two imager halves are to be treated independently, the top and bottom halves use the same row numbering scheme without contradiction.

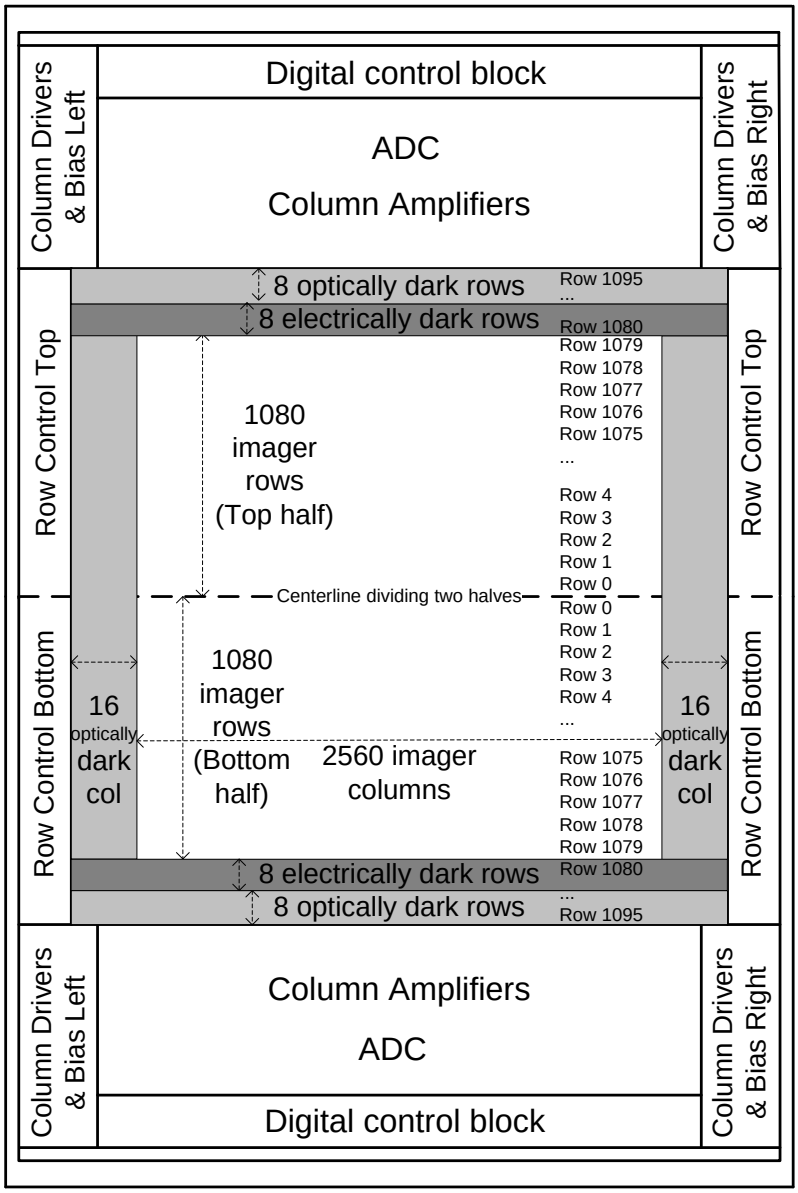


Figure 3. CIS2521 floor plan with row numbering

The optically dark rows are covered with metal so light cannot enter. The electrically dark rows are also covered with metal so light cannot enter; but in addition, all the pixels of these rows have the gates of their TX2 transistors permanently tied to AVDD. This makes them “electrically dark” as well as “optically dark”, because any charge in these dark rows (from dark current, for example) is removed via the TX2 charge dump, which is permanently active for these rows.

2.2 Device Architecture

2.2.1 Pixel Array Row and Column Numbering

Rows are numbered from 0 to 1095 in each half of the sensor, with numbers increasing moving from the center to the edge. Columns are numbered from 0 to 2591, with numbers increasing moving from left to right (as viewed from above, looking down on the sensor).

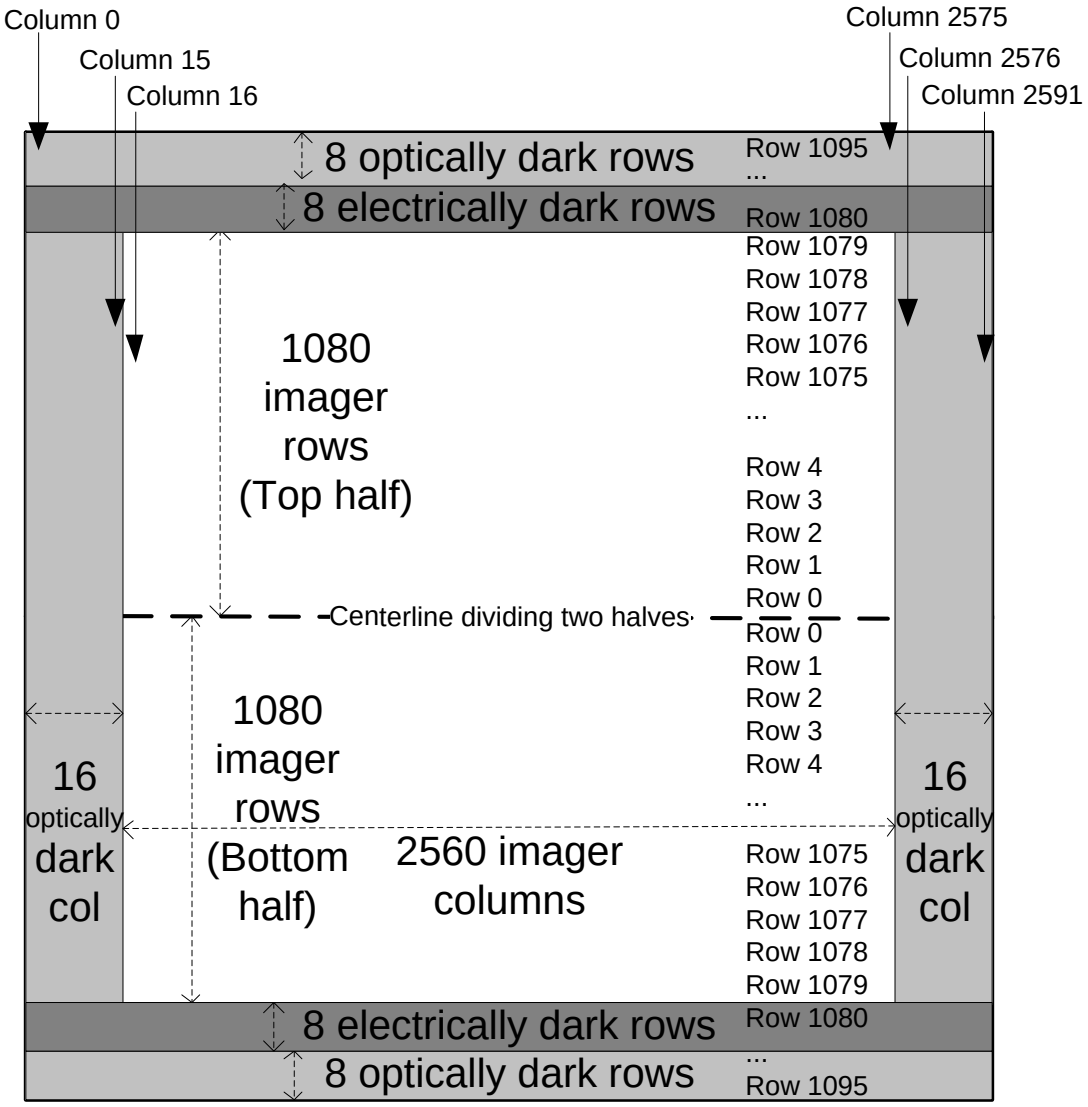


Figure 4. CIS2521AF pixel array with row and column numbering

2.2.2 Pixel Architecture

A schematic diagram of the 5T pinned photodiode pixel is shown in Figure 5. In Rolling Shutter, the pinned photodiode inside of each pixel starts to integrate charge as soon as the transfer gate TX1 is turned off. Then when the transfer gate TX1 is turned on, the integrated charge in the photodiode is dumped onto the floating diffusion node and read out as a voltage signal by the source follower. The TX2 gate serves both as a global reset gate (to mark the start of integration for Global Reset and Global Shutter modes) and as a lateral anti-blooming protection gate.

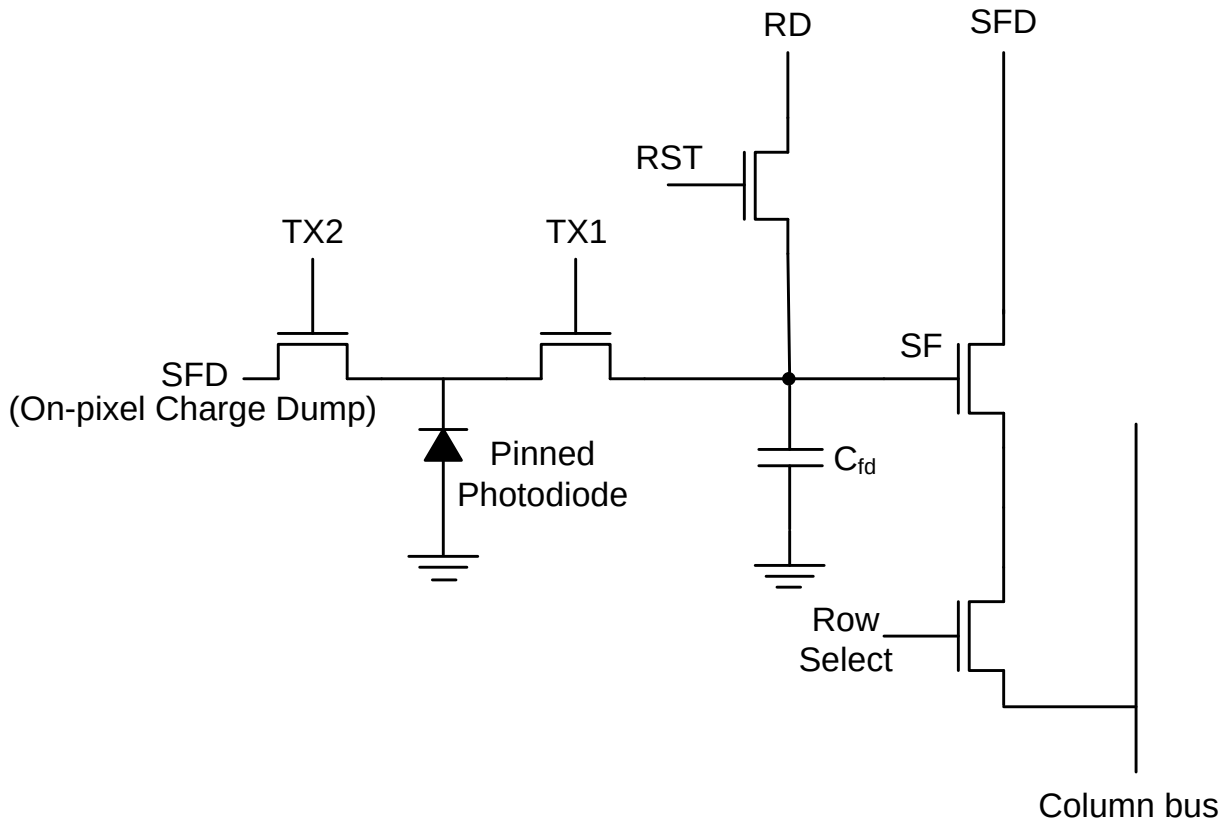


Figure 5. 5T pixel schematic

2.2.3 Column readout circuitry

Figure 6 shows the amplifier and ADC structure used in each column of the sensor. This architecture was selected to minimize the sensor read noise while maximizing dynamic range.

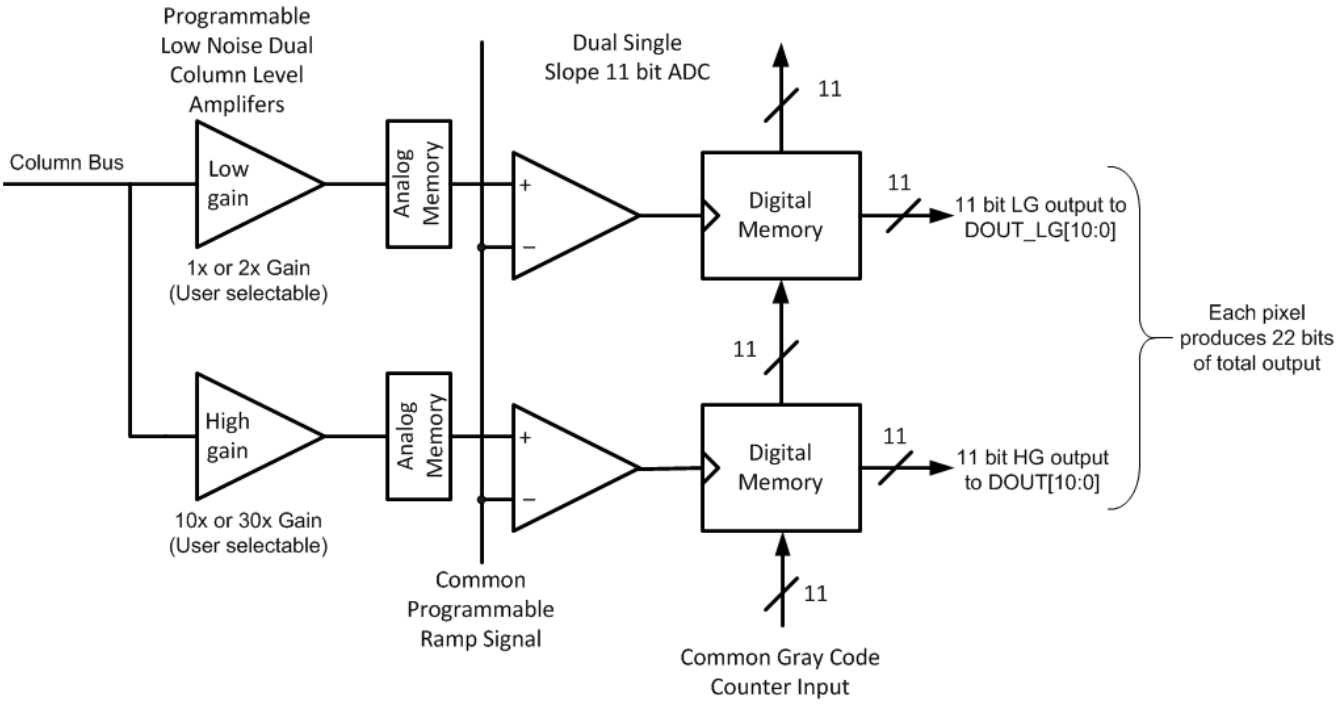


Figure 6. Column readout circuitry

There are two amplifiers per column simultaneously generating Low Gain and High Gain output signals. The gain of each amplifier is selected to either maximize the full well capacity, i.e. 1x gain, or to minimize the read noise, i.e. 30x gain. The amplifier output gain is further controlled by the settings of Register 2 bits 4 and 5. Bit 4 selects the Low Gain amplification: Bit 4 = 1 results in 1x, bit 4 = 0 results in 2x. Bit 5 selects the High Gain amplification: Bit 5 = 0 = 30x, bit 5 = 1 results in 10x. 1x for LG and 30x for HG are the defaults.

In addition to gain, the bandwidth of the column level amplifiers is also programmable via Register 2, bits [13:6]. Each column also contains two 11-bit single slope ADCs. The outputs of the amplifiers and the outputs of the ADCs are double buffered to maximize the line rate of the sensor.

The data output bus is 22 bits wide with DOUT_LG[10:0] representing the Low Gain data and DOUT_[10:0] representing the High Gain data. Because the counter input to the ADC is in Gray code, the DOUT_[10:0] and DOUT_LG[10:0] outputs will be in Gray code. The user will have to convert these outputs from Gray code to binary off-chip.

2.3 Sensor Data

After the analog pixel data is digitized, the 22-bit pixel Gray code output data is sent out through two registers to the output pads. The low gain data are delivered at the 11-bit output port DOUT_LG[10:0], and simultaneously, the high gain data are presented at the 11-bit output port DOUT[10:0].

A source synchronous output clock CLK_OUT is provided with the output data. CLK_OUT is used to register DOUT_LG[10:0] and DOUT[10:0]. CLK_OUT can be inverted or disabled via a JTAG register.

2.4 Clocking

In the packaged part, the device requires two clock inputs to be supplied by the user: SCLK on the SCLK pin and TCK on the TCK pin. Note that since the CIS2521 sensor has two halves, there are actually SCLK_TP, SCLK_BT, TCK_TP, and TCK_BT. In nearly all cases the user will have a single SCLK, but route the single SCLK to SCLK_TP and SCLK_BT, using the same source for both. Similarly, the user will typically have a single TCK source, and route this single source to the two TCK inputs (TCK_TP and TCK_BT).

2.5 SCLK

The SCLK input is the master clock to the sensor. It is a 0 to 1.8 Volt clock with a frequency range of 30 to 287 MHz.

2.6 CLK_OUT

This output clock is derived from the user-supplied input clock SCLK. CLK_OUT may have some phase shift relative to SCLK but it will be of the same frequency. The phase of the output data on the DOUT[10:0] pads and the output data on the DOUT_LG[10:0] pads is aligned to the phase of CLK_OUT.

2.7 JTAG Interface

In the packaged part, the names for the register programming pins (clock, mode select, input, output, and reset) have JTAG-style names.

Table 3: Pin Names and Description

Pin name	Package Pin number	Direction	Description
TCK_BT, TCKTP	69, 100	Input	JTAG clock TCK
TDI_BT, TDI_TP	68, 101	Input	JTAG serial data input TDI
TMS_BT, TMS_TP	65, 104	Input	JTAG mode select control TMS
TRSTB_BT, TRSTB_TP	67, 102	Input	JTAG state machine reset TRSTB
TDO_BT, TDO_TP	71, 99	Output	JTAG serial data output TDO

2.7.1 TCK

The TCK input drives the operation of the JTAG interface, which writes data into the internal registers (via the TDI pin) to control the operation of the sensor. It is also used when reading data out of the internal registers (via the TDO pin).

TCK is a 0 to 1.8 Volt clock with a frequency of 25 MHz or less.

2.7.2 Programming the Sensor

Programming the registers is done through the JTAG interface, which is controlled by an internal synchronous state machine running off TCK. TMS controls the state machine transitions. Data and address are shifted into the chip via TDI and shifted out through TDO with LSB (least significant bit) first.

2.7.3 Programming Example

The JTAG state machine and a typical programming sequence are covered in the CIS2521AF Programming Reference Manual.

3 Signals

3.1 Power and Ground Signals

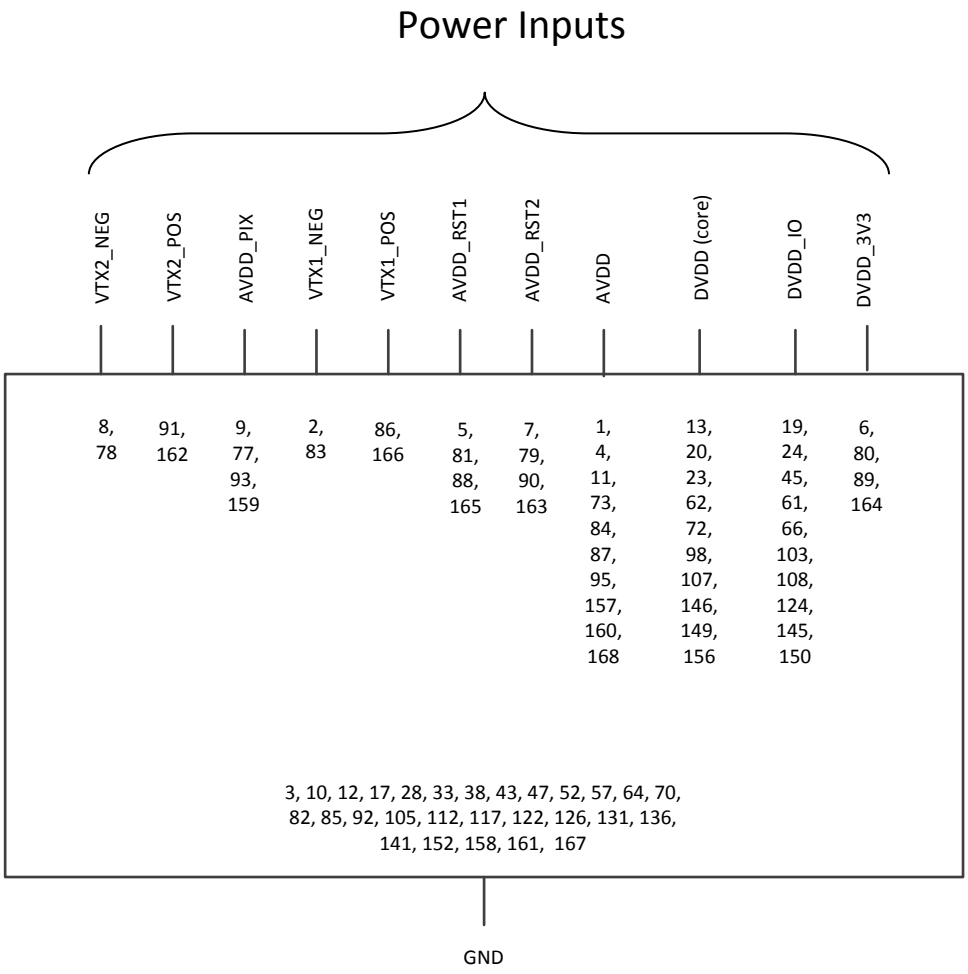


Figure 7. Power and Ground Pins

3.2 Signal Groups Diagram

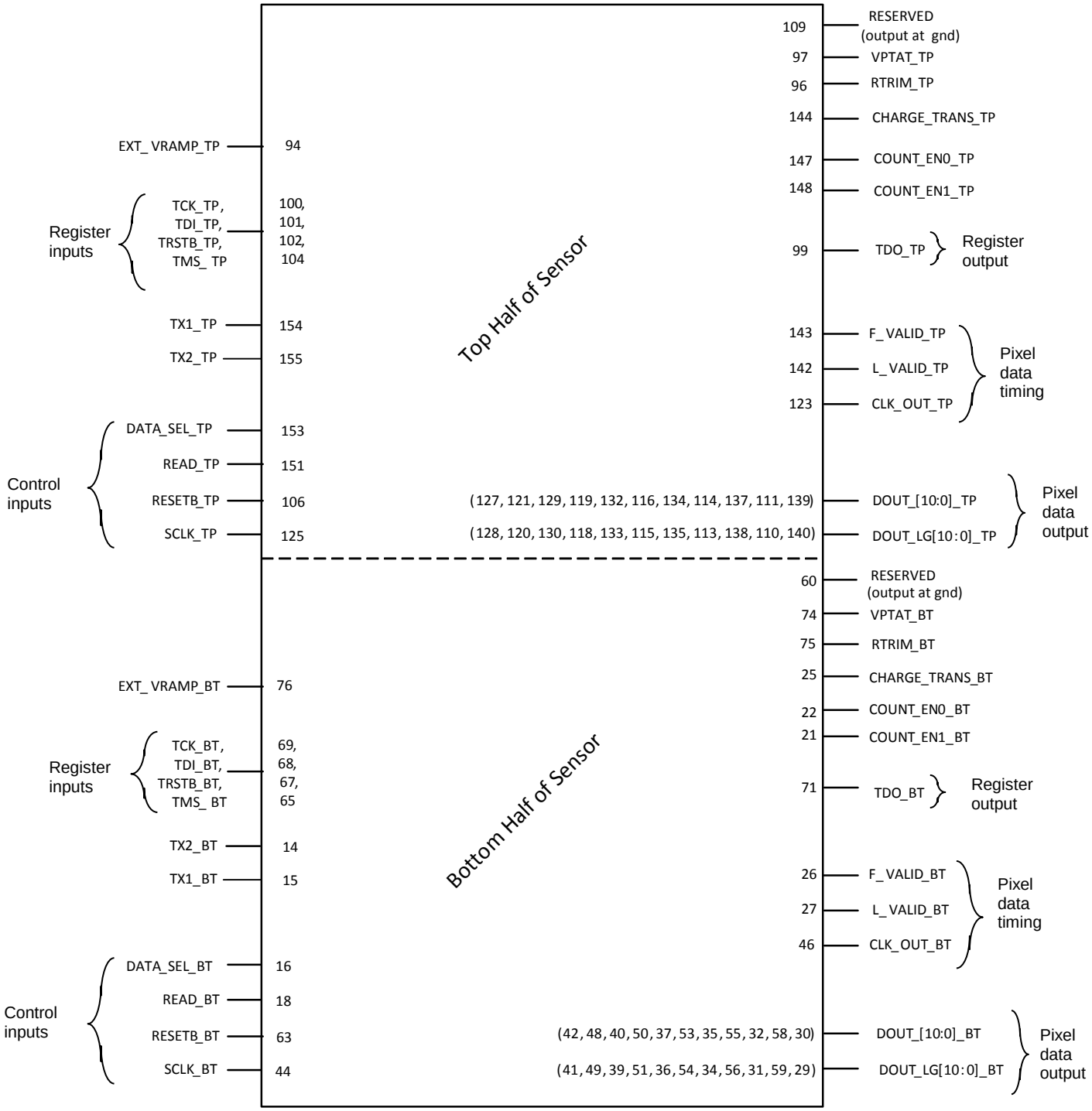


Figure 8. Signal Groups

3.3 Scientific and Standard Package Pin List

The CIS2521AF image sensor is mounted in a 168-pin ceramic leadless chip carrier (LCC package) for the FX1 Scientific, FX2 Standard, and FX4 Standard packages. For all package types, the pin list is identical. The tables shown below provide a complete description of the pin names and their functions. Note the suffix BT is appended to signal pins at the bottom of the sensor and the suffix TP is appended to signal pins at the top of the sensor.

Table 4: FX1 Scientific and FX2/FX4 Standard Package Pin List (Power and Ground)

Pin name	Pin number	Pin type	Pin description
VTX1_NEG	2, 83	Power	TX1 negative supply (Note 1)
VTX1_POS	86, 166	Power	TX1 positive supply (Note 1)
VTX2_NEG	8, 78	Power	TX2 negative supply (Note 1)
VTX2_POS	91, 162	Power	TX2 positive supply (Note 1)
AVDD_RST1	5, 81 88, 165	Power	AVDD_RST1 reset supply (Note 1)
AVDD_RST2	7, 79 90, 163	Power	AVDD_RST2 reset supply (Note 1)
AVDD_PIX	9, 77, 93, 159	Power	Pixel source follower supply (Note 1)
AVDD	1, 4, 11, 73, 84, 87, 95, 157, 160, 168	Power	AVDD analog supply (Note 1)
DVDD_3V3	6, 80, 89, 164	Power	3.3V digital supply (Note 1)
DVDD	13, 20, 23, 62, 72, 98, 107, 146, 149, 156	Power	DVDD digital core supply (Note 1)
DVDD_IO	19, 24, 45, 61, 66, 103, 108, 124, 145, 150	Power	DVDD digital I/O supply (Note 1)
GND	3, 10, 12, 17, 28, 33, 38, 43, 47, 52, 57, 64, 70, 82, 85, 92, 105, 112, 117, 122, 126, 131, 136, 141, 152, 158, 161, 167	Ground	GND common ground 0V

Note 1: Power requirements are quoted with current values for the whole imager, not just the top or the bottom half, or the left or the right side.

Note that the most of the power requirement for the chip (< 2 Watts) comes from just 4 pins:

Table 5: Power Consumption by Pin

Name	Voltage	Current	Power requirement
DVDD	1.8 Volts	290 mA (@287 MHz)	522 mW (@ 287 MHz)
DVDD_IO	1.8 Volts	270 mA (@287 MHz)	486 mW (@ 287 MHz)
AVDD	3.3 Volts	270 mA	891 mW
AVDD_PIX	3.3 Volts	25 mA	82.5 mW

Just these four pins create a power requirement of 1981.5 mW (@287 MHz). The analog supplies to the chip are invariant with SCLK frequency, but the digital supplies (DVDD and DVDD_IO) have their current consumption scale linearly with frequency. Example: at ½ the peak SCLK frequency (143.5 MHz), DVDD would need 145 mA and DVDD_IO would need 135 mA.

Table 6: FX1 Scientific and FX2/FX4 Standard Package Pin List (Signals)

Pin name	Pin number	Pin type	Signal type	Pin description
TX2_BT, TX2_TP	14, 155	Input	1.8v hstl	Global TX2 Charge dump control (Typically, this pin is only used during Global Shutter to provide the “Global TX2” charge dump pulse that marks the beginning of Global Shutter integration.)
TX1_BT, TX1_TP	15, 154	Input	1.8v hstl	Global TX1 Charge transfer control (Typically this pin is only used during Global Shutter to provide the “Global TX1” charge transfer pulse that marks the end of Global Shutter integration.)
DATA_SEL_BT, DATA_SEL_TP	16, 153	Input	1.8v lvcmos	DATA_SEL = 0 selects wavetable A for sensor readout and wavetable B for read/write access. DATA_SEL = 1 selects wavetable B for sensor readout and wavetable A for read/write access. Typically, for Rolling Shutter operation, wavetable A is always used for sensor readout, so DATA_SEL = 0 (fixed). For Global Shutter operation, DATA_SEL = 0 selects wavetable A (the GS Reset frame) and DATA_SEL = 1 selects wavetable B (the GS Data frame) so DATA_SEL is constantly

Pin name	Pin number	Pin type	Signal type	Pin description
				switching between 0 and 1.
READ_BT, READ_TP	18, 151	Input	1.8v lvcmos	External start/pause readout activities control Input.
COUNT_EN0_BT, COUNT_EN1_BT	22, 21	Output	1.8v hstl	External count and EXT_VRAMP synchronization Output. Normally ignored unless EXT_VRAMP is being used (which it typically is not).
CHARGE_TRANS_BT, CHARGE_TRANS_TP	25, 144	Output	1.8v hstl	Marker pulse indicating when data sampling of the floating node voltage is occurring for the selected row. This signal comes directly from the wavetable without any modification. In Global Shutter, the user must supply TX1, TX2, and DATA_SEL signals on external pins, and the timing of these signals should (usually) be correlated with CHARGE_TRANS (Note 1)
F_VALID_BT, F_VALID_TP	26, 143	Output	1.8v hstl	Frame valid Output. Pulses high once each frame when digital data for physical rows (i.e. dark and active imager but not pre-scan rows) appears on the DOUT/DOUT_LG pins. F_VALID rising and falling edges are controlled by the wavetable. Also called FVAL.
L_VALID_BT, L_VALID_TP	27, 142	Output	1.8v hstl	Line valid Output. Pulses once during each line readout regardless of the type of line being read out (pre-scan / dark / active imager). L_VALID rising and falling edges are controlled by the wavetable. Also called LVAL.
DOUT_LG[10]_BT DOUT_LG[10]_TP DOUT_LG[9]_BT, DOUT_LG[9]_TP DOUT_LG[8]_BT, DOUT_LG[8]_TP DOUT_LG[7],_BT,	41, 128, 49, 120, 39, 130, 51,	Output	1.8v hstl	Low gain ADC Output bits [10:0] Data output DOUT_LG[10:0] is in Gray code.

Pin name	Pin number	Pin type	Signal type	Pin description
DOUT_LG[7]_TP	118,			
DOUT_LG[6]_BT, DOUT_LG[6]_TP	36, 133,			
DOUT_LG[5]_BT, DOUT_LG[5]_TP	54, 115,			
DOUT_LG[4]_BT, DOUT_LG[4]_TP	34, 135,			
DOUT_LG[3]_BT, DOUT_LG[3]_TP	56, 113,			
DOUT_LG[2]_BT, DOUT_LG[2]_TP	31, 138,			
DOUT_LG[1]_BT, DOUT_LG[1]_TP	59, 110,			
DOUT_LG[0]_BT, DOUT_LG[0]_TP	29, 140			
DOUT_[10]_BT, DOUT_[10]_TP DOUT_[9]_BT, DOUT_[9]_TP DOUT_[8]_BT, DOUT_[8]_TP DOUT_[7]_BT, DOUT_[7]_TP DOUT_[6]_BT, DOUT_[6]_TP	42, 127, 48, 121, 40, 129, 50, 119, 37, 132,	Output	1.8v hstl	High gain of ADC Output bits [10:0]. Output data DOUT_[10:0] is in Gray code.

Pin name	Pin number	Pin type	Signal type	Pin description
DOUT_[5]_BT, DOUT_[5]_TP DOUT_[4]_BT, DOUT_[4]_TP DOUT_[3]_BT, DOUT_[3]_TP DOUT_[2]_BT, DOUT_[2]_TP DOUT_[1]_BT, DOUT_[1]_TP DOUT_[0]_BT, DOUT_[0]_TP	53, 116, 35, 134, 55, 114, 32, 137, 58, 111, 30, 139			
SCLK_BT, SCLK_TP	44, 125	Input	1.8v hstl	System clock. Input frequency between 30 MHz and 287 MHz is acceptable. Operation below 30 MHz is not recommended as the internal VRAMP voltage may become nonlinear.
CLK_OUT_BP, CLK_OUT_TP	46, 123	Output	1.8v hstl	Clock to synchronize the Data Output
Reserved	60, 109	Output	1.8v hstl	Output fixed at 0 Volts
RESETB_BT. RESETB_TP	63, 106	Input	1.8v lvcmos	Active low reset Input
TMS_BT, TMS_TP	65, 104	Input	1.8v lvcmos	JTAG mode select control
TRSTB_BT, TRSTB_TP	67, 102	Input	1.8v lvcmos	JTAG reset (active low)
TDI_BT, TDI_TP	68, 101	Input	1.8v lvcmos	JTAG serial data Input

Pin name	Pin number	Pin type	Signal type	Pin description
TCK_BT, TCK_TP	69, 100	Input	1.8v lvcmos	JTAG clock (should be less than 25 MHz)
TDO_BT. TDO_TP	71, 99	Output	1.8v hstl	JTAG serial data Output
VPTAT_BT, VPTAT_TP	74, 97	Output	Analog	Temperature sensor Output (Note 2)
RTRIM_BT, RTRIM_TP	75, 96	Output	Analog	External current reference resistor pins. Should have a 12.28 KΩ resistor connected to this pad at one end and ground at the other.
EXT_VRAMP_BT, EXT_VRAMP_TP	76, 94	Input	Analog	Optional external VRAMP input that is used in place of the internal voltage ramp when JTAG Register 2 bit 16 = 1. Normally the internal VRAMP is used and this pin is either left as a no connection or tied to ground. If it is used, the ADC ramp power requirements are: voltage (from 1.0V to 2.5V) current (20mA)
COUNT_EN0_TP, COUNT_EN1_TP	147, 148	Output	1.8v hstl	External count and EXT_VRAMP synchronization Output. Normally ignored unless EXT_VRAMP is being used (which it typically is not).

Note 1: CHARGE_TRANS is an output provided by the wavetable that pulses once each row readout. For the default and BAE-recommended wavetables (see “MAN 0102”, the CIS2521AF Programming Manual), the time to read out a row of pixels is equal to 2624 SCLKs. CHARGE_TRANS is high for 2319 SCLKs and low for 305 SCLKs. At full speed (287 MHz) this means that CHARGE_TRANS is low for 1.06 µseconds.

The CHARGE_TRANS signal does not directly control anything. It is a marker signal for the user to indicate when data sampling is occurring. When CHARGE_TRANS is high, data sampling of the pixel floating diffusion node voltage is occurring, or will shortly occur, or has recently occurred. When CHARGE_TRANS is low, data sampling of the pixel floating diffusion node voltage has already taken place and is in no danger of being disturbed.

This is relevant in Global Shutter, because, unlike Rolling Shutter, the user must define the exposure time by inputting voltage pulses on the chip’s external pins for TX1 and TX2. A pulse on TX2 marks the beginning of integration (because it clears out the pixel photodiode charge) while a pulse on TX1 marks the end of integration (because it transfers the pixel photodiode charge to the floating diffusion node to be read out).

These pulses go directly to the pixel, and therefore should ideally occur during the CHARGE_TRANS low period when such pulses will not disturb the floating diffusion voltage sampling (because it has already

occurred). If the user fails to do this, the row of data that sees a TX1 or TX2 voltage transition during the CHARGE_TRANS high period may be corrupted.

The function of the TX1 and TX2 pulses is to empty the pixel photodiode of charge. The TX1 pulse empties the pixel photodiode of charge by transferring it to the pixel floating diffusion. The TX2 pulse empties the pixel photodiode of charge by transferring it to the on-pixel charge dump. Inadequate charge transfer is called “lag” and there are typically 3 ways to improve lag:

1) Raise the relevant positive voltage for the transfer transistor (i.e. raise VTX1_POS or VTX2_POS)
2) Extend the TX1 or TX2 pulse time
3) Increase the temperature of the sensor

It is possible that the CHARGE_TRANS low period will be inadequate to provide sufficient charge transfer, and so lag will result. A line time is equal to 2624 SCLKs, and CHARGE_TRANS goes high on SCLK 3 and falls on SCLK 2322. As previously mentioned, this means that CHARGE_TRANS is high for 2319 SCLKs (from SCLK 3 to SCLK 2322) and low for 305 SCLKs (from SCLK 2322 to 2624, plus 3 more SCLKs from the next line time).

The measurement events where the risk of data corruption is present occur at SCLK 1145 and SCLK 2299. Since both these times are when CHARGE_TRANS is high, the simplest advice on TX1 and TX2 pulses is to time the TX1 and TX2 pulses to the CHARGE_TRANS low period.

If the rising edge of TX1 (or TX2) is synchronous with the falling edge of CHARGE_TRANS (SCLK 2322), and the falling edge of TX1 (or TX2) is synchronous with the rising edge of CHARGE_TRANS (SCLK 2 of the next line time), this time is 305 SCLKs. At 287 MHz, 305 SCLKs equates to 1.06 microseconds.

In some circumstances (particularly at cold temperatures like -40 degrees C), 1.06 microseconds may not be enough and lag will become evident. In this case, it is recommended to go beyond the “pulse only during the CHARGE_TRANS low period” limit and extend the TX1 (or TX2) pulse for 1.5 microseconds. Even at cold temperatures, 1.5 microseconds ought to be enough. So the rule would be:

1) Begin the TX1 (or TX2) pulse when CHARGE_TRANS goes low (SCLK 2322)
2) End the TX1 (or TX2) pulse either
    a. When CHARGE_TRANS goes high (Low SCLK frequency case)
    b. When 1.5 microseconds have elapsed (High SCLK frequency case)

    (Choose whichever is longer in duration.)

At an SCLK frequency of 287 MHz, 1.5 microseconds equates to 431 SCLKs. So if the above advice is followed for the 287 MHz case, TX1 (or TX2) would rise at SCLK 2322 and would fall 431 SCLKs later at SCLK 129 (or the next line time). Note that SCLK 129 is still quite far from SCLK 1145 (or 2299) where the measurement events take place, so this following this advice will defeat lag at cold temperatures without causing data corruption.

TX1 (or TX2) pulses occurring when pre-scan rows are being read out are a special case. If the row being read out is a pre-scan row, the TX1 (or TX2) will not be connected to any physical row of pixels, and so interference of floating diffusion node voltages is not a concern. Figure 13 and Figure 20 in this datasheet are examples of this.

Another example (where the risk of data corruption is not present) is when Global Shutter is set up to loop on multiple Reset frames prior to reading out the Data frame in order to get an extended exposure time. In this case, the start of the integration period (indicated by a TX2 pulse) could be during a CHARGE_TRANS high period if it occurred during any of the Reset frames except the one that immediately precedes the

Data frame. This is because the final image will be constructed from the Data frame and its immediately preceding Reset frame. If a line of data was corrupted in one of the earlier Reset frames, it makes no difference since that data will not be used to construct the final image. This consideration is also at work when, instead of pulsing the TX2, the user decides to hold TX2 high and mark the start of integration by dropping TX2. This is seen in Figure 16 and Figure 18. In those figures, the TX2 signal goes from high to low much earlier than the Reset frame that immediately precedes the Data frame, and so there is no risk of inducing artifacts in the final image.

In Global Shutter, DATA_SEL is the input that makes the transition between the wavetables A and B. With DATA_SEL = 0, the sensor reads out according to the pattern of wavetable A, and with DATA_SEL = 1, the sensor reads out according to the pattern in wavetable B. The CIS2521AF registers, including the wavetable registers, are loaded with default values at power-up (and also when RESETB = 0). These default values (and also the BAE-recommended ones to program in that are in the CIS2521AF Programming Manual) assume that wavetable A is used for the Global Shutter Reset frame and wavetable B is used for the Global Shutter Data frame. Therefore, in order for the sensor to function in Global Shutter, the user must frequently be changing DATA_SEL from 0 to 1 and from 1 to 0.

The normal row readout pattern in a frame is: pre-scan rows, followed by dark rows, followed by the active imager rows. If there are pre-scan rows, making the DATA_SEL transition (0 = >1 or 1 = >0) and TX1 pulse during the pre-scan row readout is the safest: even if you don't make these actions during the CHARGE_TRANS low period, it doesn't matter since pre-scan rows (i.e. physically non-existent rows) are being read out.

In the most difficult case, when there are only active imager rows in the frame, problems can easily occur. Timing the DATA_SEL transition is done by monitoring the FVAL signal which drops briefly when a completed frame is read out at the digital outputs (DOUT/DOUT_LG pins). That is, FVAL dips briefly when the digital data for the last row in the frame appears on the DOUT/DOUT_LG pins. The analog data at the pixel level for this last row of the frame was read out 2 line times earlier (because pixel data readout is a three line time process: analog pixel readout, analog to digital conversion in the column amplifiers, and digital readout at the DOUT/DOUT_LG pins). The DATA_SEL transition should therefore have occurred 2 line times prior to the dip in the FVAL signal. To avoid complications of this sort, it is best to include some pre-scan lines in your frames when doing Global Shutter. Problems can be avoided with a simple formula:

1) Have a small number (at least 4) of pre-scan lines in each Global Shutter frame.
2) Make the DATA_SEL 0 = > 1 and 1 = >0 transitions during the middle of the pre-scan period.
3) Make the TX1 pulse in the pre-scan period that marks the beginning of the Data frame (here assuming a standard readout order of pre-scan => dark => active imager).
4) The TX2 pulse can occur at any time, but must occur during a CHARGE_TRANS low period.
   (This rule can be ignored if the readout arrangement includes multiple Reset frames prior to the Data frame, and the start of integration marked by TX2 occurs in one of the Reset frames other than the one immediately preceding the Data frame. This rule can also be avoided if integration times less than one line time are needed and the TX1 pulse takes place during pre-scan readout. In that case, the TX2 pulse will also take place during pre-scan readout and therefore have no effect on the imager regardless of the CHARGE_TRANS state.
5) For added (redundant) protection, the TX1 pulse can be limited to a CHARGE_TRANS low period, and the DATA_SEL transitions can be synchronous with a falling edge of CHARGE_TRANS low. The DATA_SEL 0=>1 transition and the TX1 rising edge would also be synchronous.

Note 2: VPTAT (Voltage Proportional to Absolute Temperature) should output a voltage over 2 Volts at room temperature which will vary linearly with temperature. The user should calibrate this output against an external temperature measuring device (e.g. a thermocouple on the back of the imager). A typical coefficient of voltage change to temperature change is 6.5 mV per degree Celsius.

4 Power Down and Use of READ pin

4.1 Pause/Resume using READ pin

The READ pin switching to 0 will glitchlessly stop SCLK when JTAG Register 2 (mode register) bit 21 is 0, resulting in a “zero activity” pause operation. All sensor activities other than JTAG write or reset will be frozen. The assertion of the READ pin to 1 will cause SCLK to resume normal sensor operation. While the clock is stopped, it is possible that the voltage ramp generator will lose synch. The voltage ramp generator will take up to 65 row periods to stabilize.

4.2 Reset using READ pin

When JTAG Register 2 (mode register) bit 21 is 1, READ resets the sensor state (except the JTAG register values will not be forced back to their default values). This behavior is necessary to either:

a. start operation from a controlled start point, or
b. start synchronously for pseudo single port readout operation.

4.3 External trigger using READ pin

When JTAG Register 2, bit 23, is 1, it overrides the setting of bit 21 as described above and modifies the behavior of the READ pin. This is called external trigger mode. In this mode, the READ pin is sampled at the end of the line time. A change in the value of READ before and after the sample qualifies as a transition on READ.

5 Shutter Operation

5.1 Rolling Shutter Readout Mode

Rolling Shutter is the standard readout method for CMOS image sensors. When READ is asserted in Rolling Shutter mode, one row at a time is sequentially processed until the frame is completely read out. In video readout mode, i.e. when READ is always asserted, frames are continuously read out, separated only by a programmable frame blanking time. Note that the frame blanking time is determined by the number of pre-scan lines in each image. Readout of each row consists of four separate operations. The first operation is resetting the floating diffusion nodes in each pixel. The second operation is reading the reset voltage out via the source follower transistor in each pixel. The third operation is transferring charge from the pinned photodiode to the floating diffusion node, via TX1, and the last operation is reading out the signal voltage. At the edge of the array, column parallel circuitry amplifies, subtracts, and digitizes the row data. The difference between the reset voltage the signal voltage is a form of correlated double sampling (CDS). CDS removes kTC, i.e. reset, noise on the floating diffusion node, and suppresses the source follower 1/f noise. This readout mode achieves the lowest read noise available for the CIS2521AF.

The CDS operation in Rolling Shutter mode is illustrated in Figure 9. The floating diffusion voltages of rows N-M, N-M+1, and N are shown. The reset sample for each row is S1 and the data sample for each row is S2. The final pixel value is the difference between S2 and S1.

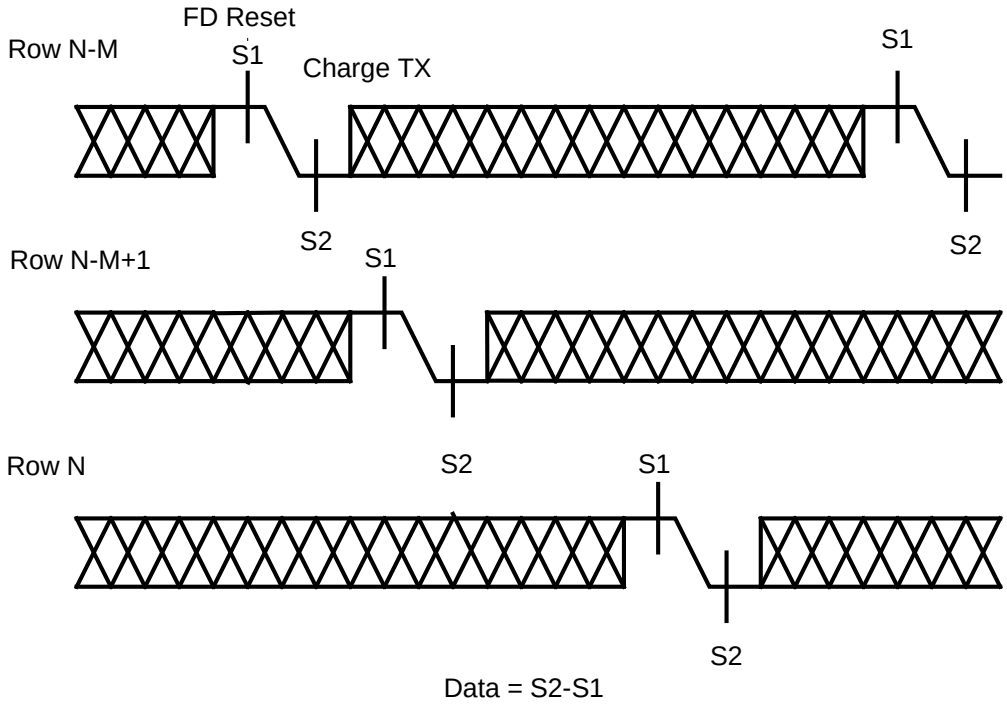


Figure 9. CDS Operation in Rolling Shutter Mode

In Rolling Shutter readout, each row in the sensor integrates photo-charge for the same amount of time but the exact time interval is different. Moreover, the integration interval for row N+1 is shifted by one line time in comparison to row N. Figure 10 illustrates this effect.

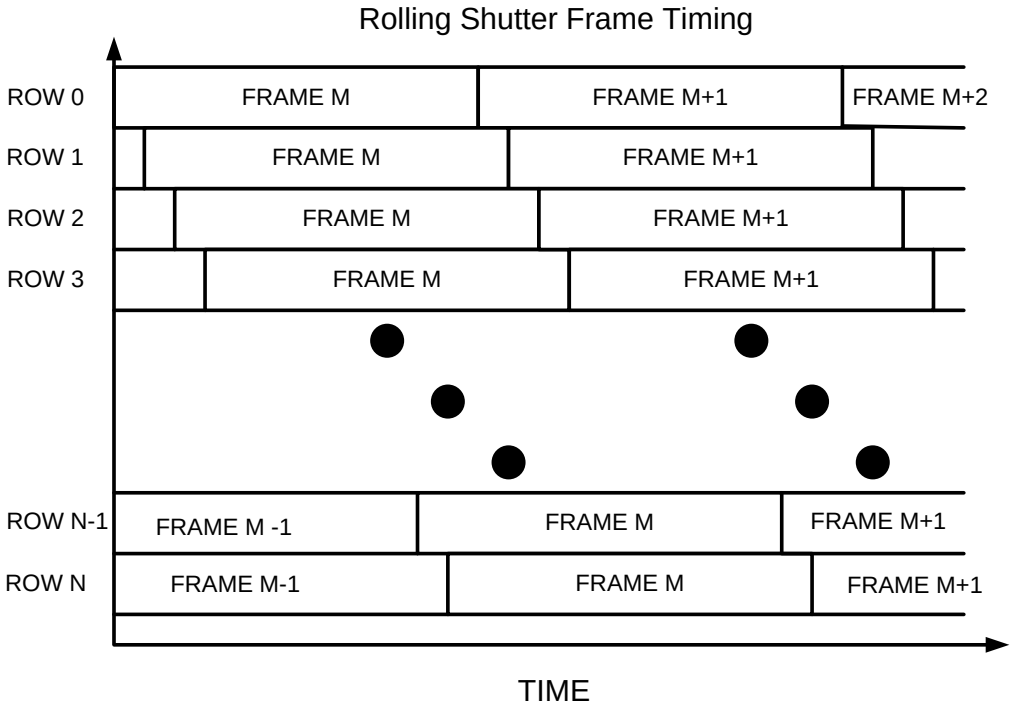


Figure 10. Integration during Rolling Shutter Mode

5.1.1 Seamless change of integration time in Rolling Shutter readout

Seamless change of integration time in Rolling Shutter readout mode is implemented on this sensor to allow standard auto exposure algorithms to be implemented in a camera. This operation is always active in Rolling Shutter readout mode. Seamless change of integration time is implemented in the sensor by forcing the integration time of each row in each frame to be the same. This enables smooth video output when integration time is used as an electronic shutter.

5.1.2 Basic Rolling Shutter Mode

Frame and line timing diagrams of the CIS2521AF sensor in various operating modes are shown next.

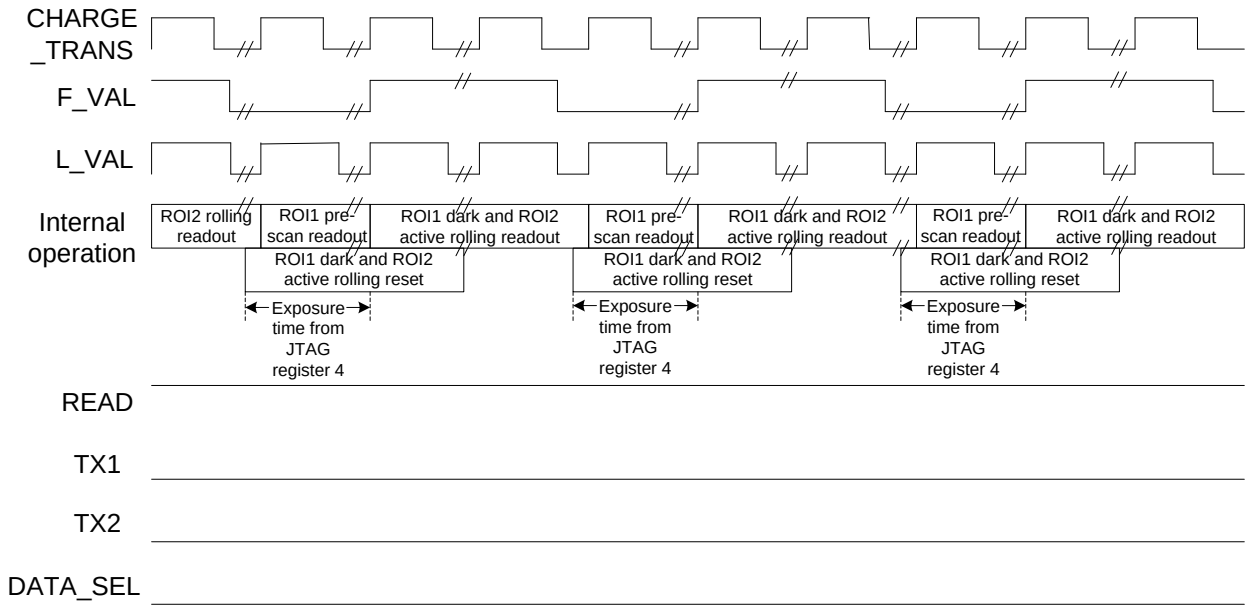


Figure 11. Basic Rolling Shutter Mode

5.1.3 Pause/Resume using READ pin

The READ pin switching to “0” will stop SCLK without glitches when JTAG register 2 (mode register) bit 21 is “0” resulting in a “zero activity” pause operation. All sensor activities other than JTAG operation or reset will be frozen. The assertion of the READ pin to “1” will cause SCLK to resume normal sensor operation. While the clock is stopped, it is possible that the internal voltage ramp generator will lose synchronization. The voltage ramp generator will take up to 65 row periods to stabilize.

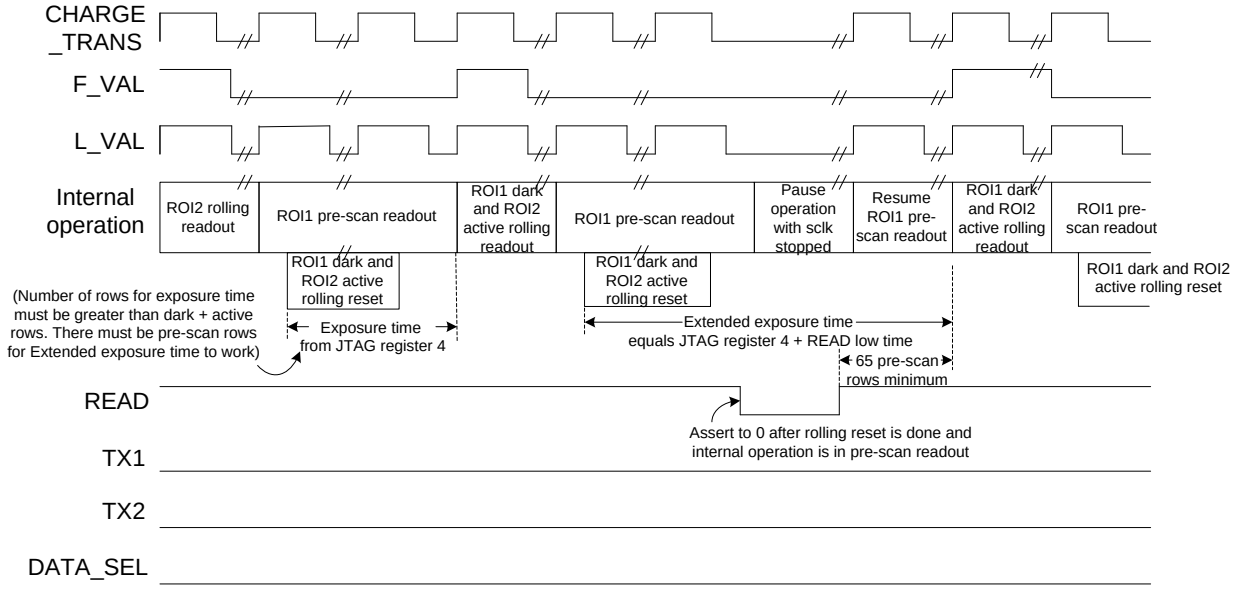


Figure 12. Rolling Shutter Mode using READ pin to extend exposure time. (Register 2, bit 21=0)

5.1.4 Rolling Shutter External trigger using READ pin

When JTAG register 2 bit 23 is 1, it overrides the setting of bit 21 as described in the previous section and modifies the behavior of the READ pin. With bit 23 = 1, the sensor is in external trigger mode, and the READ pin is the input for the external trigger. In this mode, the READ pin is sampled at the end of the line time. A change in the value of READ before and after the sample qualifies as a transition on READ. Figure 13 and Figure 14 use external trigger. In Figure 13, Rolling Shutter exposure is controlled by READ.

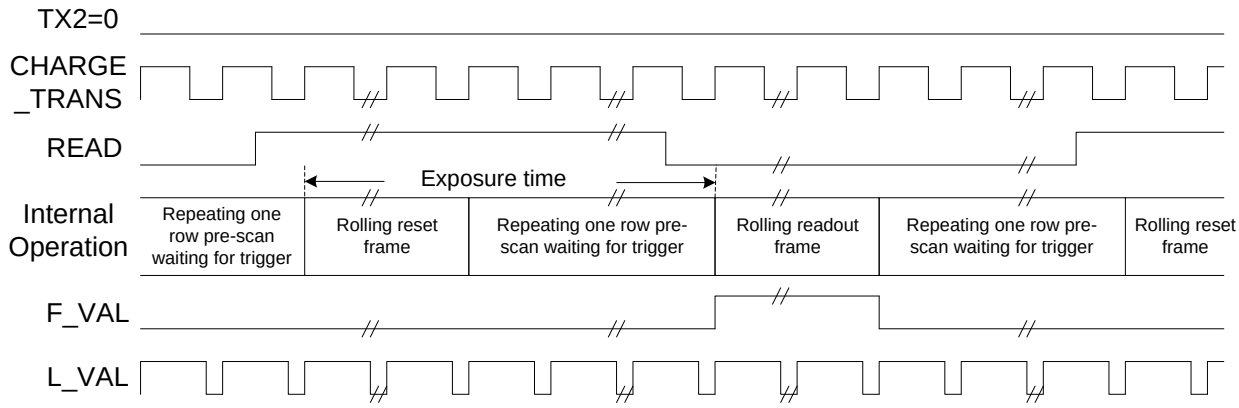


Figure 13. Rolling Shutter Mode with External Trigger, (Register 2, bit 19=0, bit 23=1)

In Figure 14, Rolling Shutter exposure is controlled by READ and TX2

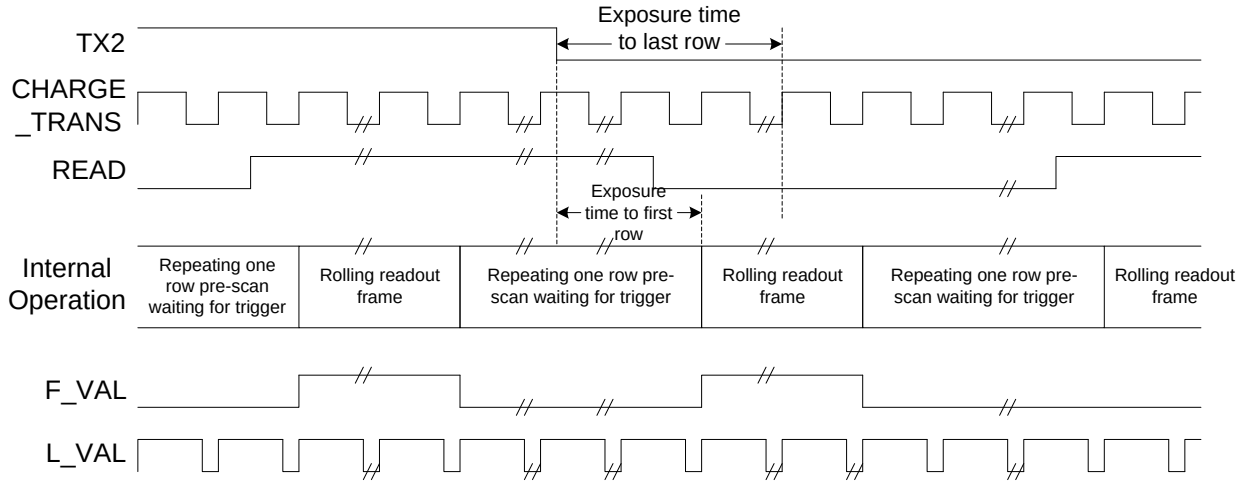


Figure 14. Rolling Shutter Mode with External Trigger, (Register 2 bit 19=1 and bit 23=1)

In this mode, the start of integration time for all pixels in the array is the falling edge of TX2 (since TX2 operates globally on all pixels). The ending time of integration differs row by row, controlled by the Rolling readout frame. If a scene under consideration is lit by a strobing light source that flashes after the fall of TX2 but before the start of Rolling readout, the scene will be free of the motion artifacts that can otherwise occur in standard Rolling Shutter. Because of this mode's action to suppress motion artifacts (when used in conjunction with a strobing light source), this mode is sometimes called "Global Reset" (to evoke the motion artifact immunity of Global Shutter, even though this mode is actually Rolling Shutter).

5.2 Global Shutter Readout Mode

5.2.1 Global Shutter Readout Mode Pixel Control

Table 7: Global Shutter Control

Name	Package Pin number	Direction	Description
TX1_BT, TX1_TP	15, 154	Input	Global Shutter readout mode charge transfer pulse.
TX2_BT, TX2_TP	14, 155	Input	Exposure control / charge dump signal. Although not generally used for Rolling Shutter (see Figure 11, Figure 12, and Figure 13), this signal can have the same exposure control function in Rolling Shutter mode (see Figure 14).

Note: Please refer to the CIS2521AF Programming Manual for additional information.

5.2.2 Global Shutter Operation

Global Shutter operation allows every pixel in the sensor to integrate charge during the same time period. This minimizes motion artifacts when compared with Rolling Shutter operation. The CIS2521AF performs Global Shutter using TX1 (transfer charge from pinned photodiode to floating diffusion) and TX2 (dump charge from pinned photodiode) to simultaneously control the end and start of integration respectively. Both TX1 and TX2 are active high, i.e. they transfer or dump charge when high.

In order to achieve low noise readout, correlated double sampling (CDS) must be performed to mitigate the effects of reset and 1/f noise in each pixel. Due to the global operation of TX1, the typical Rolling Shutter-type readout method (scrolling reset and then readout of each line) cannot be used to perform CDS. Therefore correlated quadruple sampling (CQS) is used to minimize read noise. CQS requires that the sensor be read out twice to construct each image frame. Moreover, a Reset frame and a Data frame are required for each image and the final image is created by subtracting the Reset frame from the Data frame. The first readout, i.e. the Reset frame, is a measurement of the kTC noise charge on the floating diffusion in each pixel. The second readout, i.e. the Data frame, is a measurement of the charge transferred from the pinned photodiode onto the floating diffusion.

Figure 15 illustrates the operation of CQS. S1r and S2r are reset samples collected during a Reset frame, and S1d and S2d are data samples collected during a Data frame. During a Reset frame each row within the ROI is read out sequentially. When a given row is selected all of the floating diffusion capacitances in that row are first hard reset to RD via the reset transistor in each pixel. Then, while the reset transistor is on, S1r samples the pixel voltage. Then the reset gate is turned off and S2r samples the floating diffusion, i.e. the noise charge. After all of the rows in the Reset frame are read out, charge can be transferred from the pinned photodiode to the floating diffusion capacitance in each pixel. After charge is transferred to the floating diffusion capacitance a Data frame can be collected. Similar to the readout of a Reset frame, a Data frame is read out sequentially row by row. While a given row is selected, all of the floating diffusion capacitances in that row are first sampled via S1d. Then the reset transistor in each pixel is turned on and S2d samples the pixel voltage. Finally the Reset frame is subtracted from the Data frame, external to the sensor, forming the image S1d-S2r. Note that this assumes that S1r and S2d are the same value, which is

only true if RD is noiseless. Therefore, the noise voltage on RD is critical to the final read noise of the sensor in Global Shutter operation.

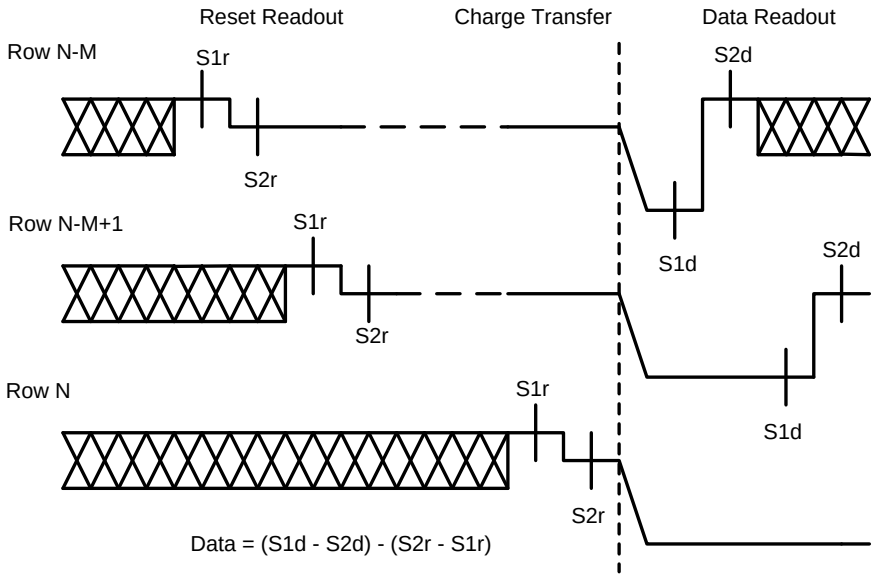


Figure 15. Correlated quadruple sampling operation

The following sections discuss Global Shutter operation in more detail and explain Reset frame and Data frame readout.

5.2.3 Reset frame readout

In Global Shutter mode, reset readout occurs when the DATA_SEL is low and the READ is high. Each Reset frame begins at the first row of ROI_1 and ends with the last row of ROI_2. For example, if ROI_1 start = 2047 and ROI_1 stop = 1080 then 952 pre-scan lines and 16 optically dark lines are sequentially read out from ROI_1. If ROI_2 start = 11 and ROI_2 stop = 1070 then the row counter counts up and 1060 active rows are read out of the sensor in ROI_2. Note that after row 1080 is read out of ROI_1 then the next row, i.e. the first row of ROI_2, is row 11. If DATA_SEL is held low and READ is held high, Reset frames will continue to be generated by the sensor and the row counter will continuously cycle through the row values in the current ROIs.

In video mode every Reset frame needs to be followed by a Data frame. Note that just like Rolling Shutter mode, the frame blanking time is determined by the number of pre-scan lines in each image. When switching between a Reset frame and a Data frame, DATA_SEL should be toggled during the frame blanking period.

5.2.4 Data frame readout

In Global Shutter mode, data readout occurs when the DATA_SEL is high and the READ is high. Each Data frame begins at the first row of ROI_1 and ends with the last row of ROI_2. For example, if ROI_1 start = 2047 and ROI_1 stop = 1080 then 952 pre-scan lines and 16 optically dark lines are sequentially read out from ROI_1. If ROI_2 start = 11 and ROI_2 stop = 1070 then the row counter counts up and 1060 active rows are read out of the sensor in ROI_2. Note that after row 1080 is read out of ROI_1 then the next row, i.e. the first row of ROI_2, is row 11. If DATA_SEL is held high and READ is held high, Data frames will continue to

be generated by the sensor and the row counter will continuously cycle through the row values in the current ROIs. To perform correlated quadruple sampling, a Reset frame must be read out before each Data frame. When performing long integrations (greater than one frame time), multiple Reset frames may occur before a Data frame. For correct CQS sampling, the pair of frames chosen for CQS should be the Data frame and the Reset frame that occurs just before it.

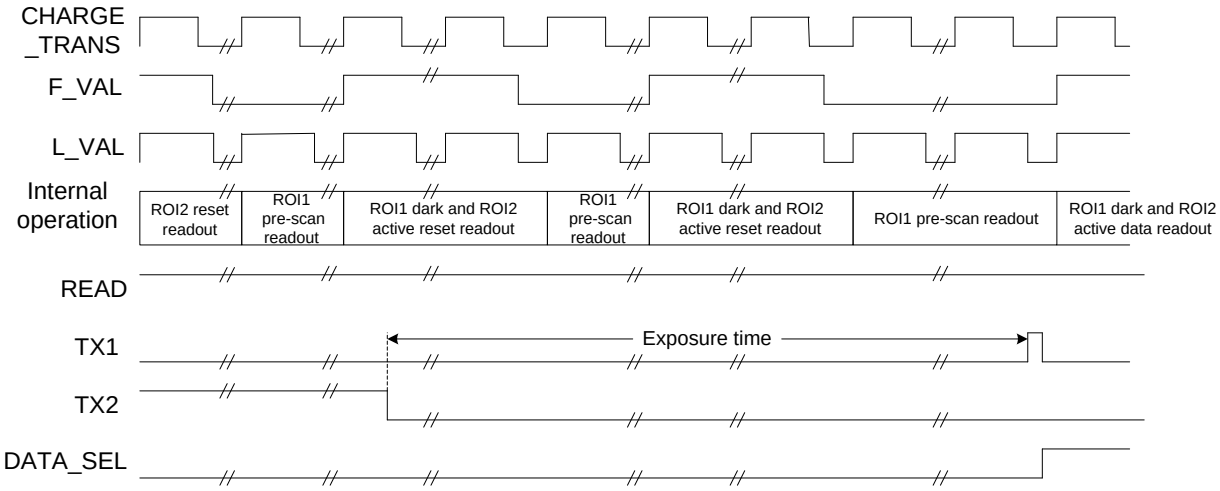


Figure 16. Basic Global Shutter Mode

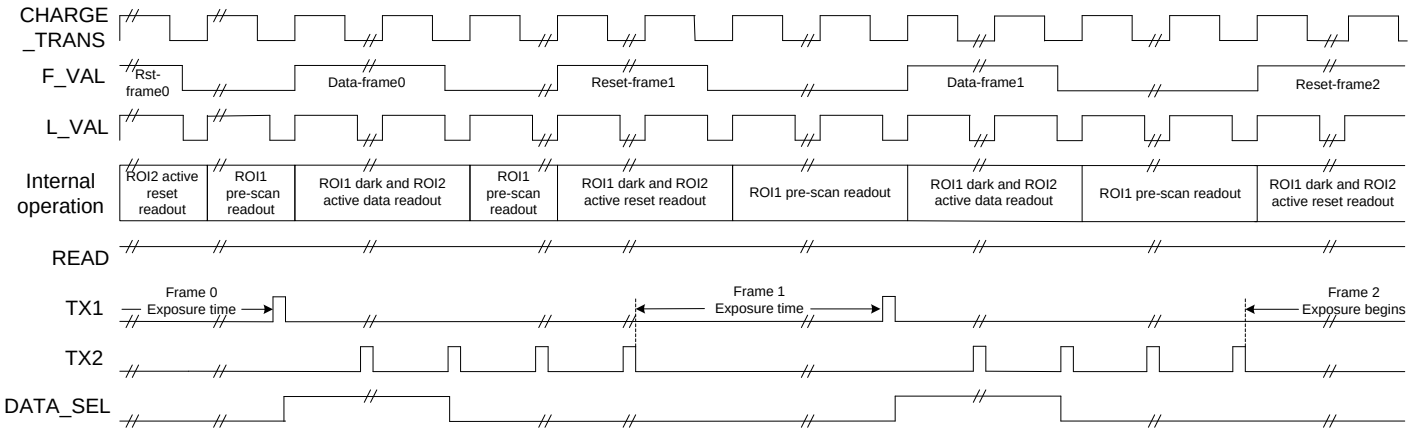


Figure 17. Basic Global Shutter Mode, Short Exposure (Similar to Figure 16 but with more details)

Note: Figure 17 and Figure 18 show an identical readout mode (Basic Global Shutter Mode) with the only difference being that Figure 17 gives the example of a short exposure time and Figure 18 has a long exposure time.

The signals that are different are F_VAL (Figure 17 has one Reset frame preceding the Data frame, Figure 18 has two) and TX2 (Figure 17 has TX2 pulsed during the CHARGE_TRANS low period in each row readout, and Figure 18 has TX2 continuously on or continuously off).

Previously it has been stated that TX2 should be pulsed during the CHARGE_TRANS low time to avoid banding artifacts in the image. Since the Global Shutter final image is constructed from the Data frame and the immediately preceding Reset frame, any TX2 activity during this immediately preceding Reset frame must be pulsed, and this is shown in Figure 17.

In Figure 18, however, the last falling edge of TX2 is not in the immediately preceding Reset frame (Reset frame 1), but rather in the Reset frame before that (Reset frame 0). TX2 activity in this region cannot induce any banding artifacts in the final Global Shutter image, since only data in the immediately preceding Reset frame (Reset frame 1) is used to create the final image.

Therefore, pulsing TX2 in Global Shutter is not necessary as long as there is no TX2 activity when active imager rows are being read out for a Data frame or its immediately preceding Reset frame. Having TX2 continuously on during either of these periods would produce banding artifacts. A time period when active imager rows are being read out roughly corresponds to when F_VAL is high, though F_VAL is high for both dark rows and active imager rows (= “physical rows”), and F_VAL (by default) has a 2 row time delay in its rise and fall times from when the physical rows begin and end their frame readout.

Of course, all complications can be avoided by pulsing TX2 during the CHARGE_TRANS low time regardless of the exposure time. However, pulsing TX2 incurs a cost in current consumption. In Low power applications, TX2 may therefore avoid pulsing for long exposure times, as is shown in Figure 18 below.

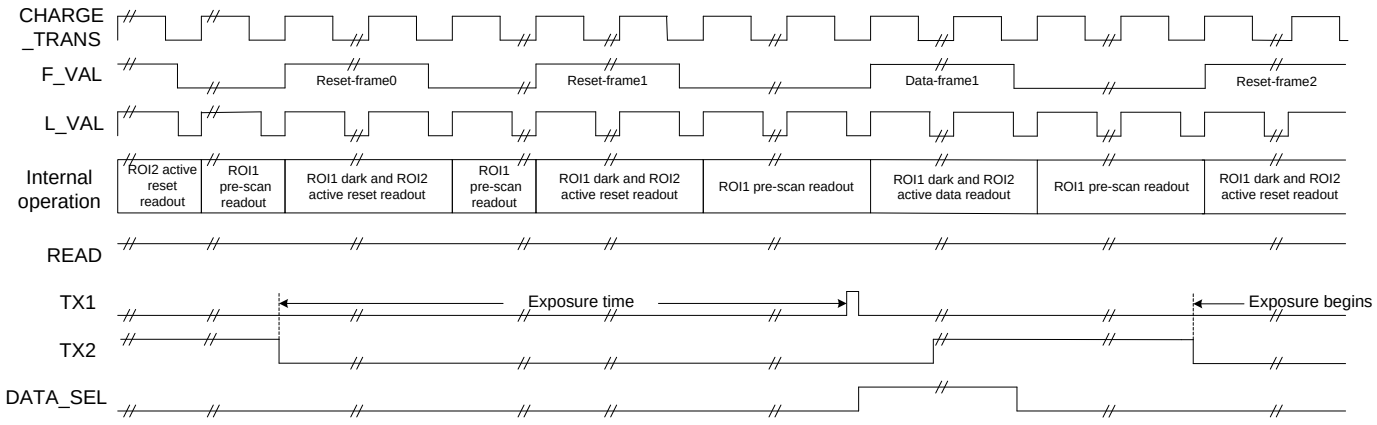


Figure 18. Basic Global Shutter Mode, Long Exposure (Similar to Figure 16, but with more details)

5.2.5 Global Shutter Pause/Resume using READ pin

The READ pin switching to “0” will stop SCLK without glitches when JTAG register 2 (mode register) bit 21 is “0” resulting in a “zero activity” pause operation. All sensor activities other than JTAG operation or reset will be frozen. The assertion of the READ pin to “1” will cause SCLK to resume normal sensor operation. While the clock is stopped, it is possible that the internal voltage ramp generator will lose synchronization. The voltage ramp generator will take up to 65 row periods to stabilize.

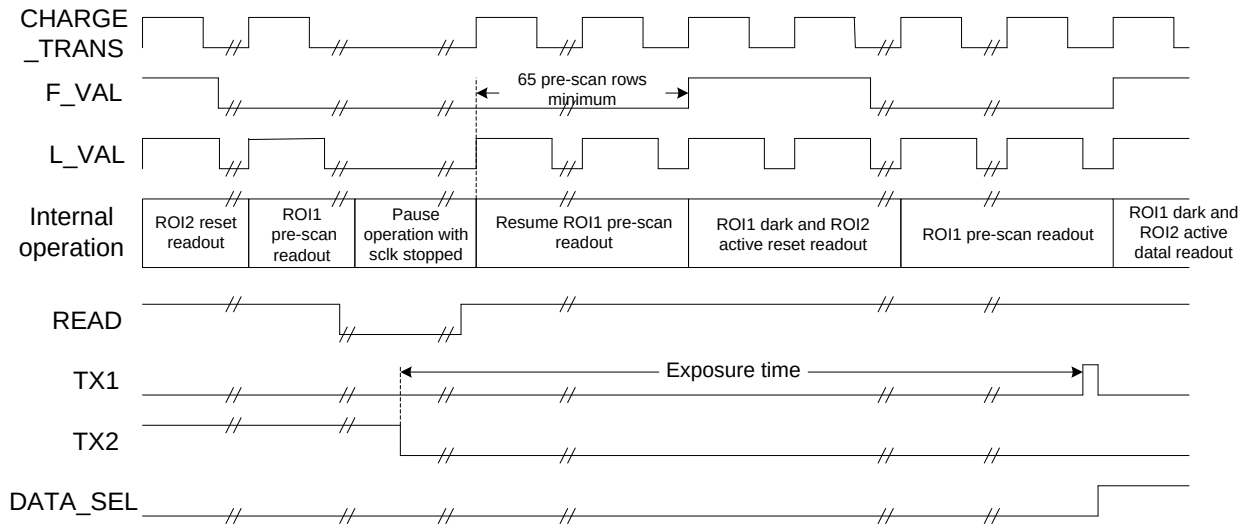


Figure 19. Global Shutter Mode using READ pin to extend exposure time

5.2.6 Global Shutter external trigger

In this mode, each transition of the READ pin causes one and only one frame of either reset or data operation (depending on the value of DATA_SEL) before the sensor goes into an “idling” state where only one virtual row is continuously being accessed. In the “idling” state, the sensor is waiting for the next transition on READ. While the sensor is “idling”, external control signals TX1 and TX2 can be applied to precisely control the start and duration of the frame exposure. The response time of the sensor to a READ transition is one row time, i.e. the amount of time required to switch from the virtual row to a valid row.

In Figure 20, Global Shutter exposure is controlled by TX1 and TX2 pulses, as usual, but the timing of Reset and Data frame readouts is controlled by READ.

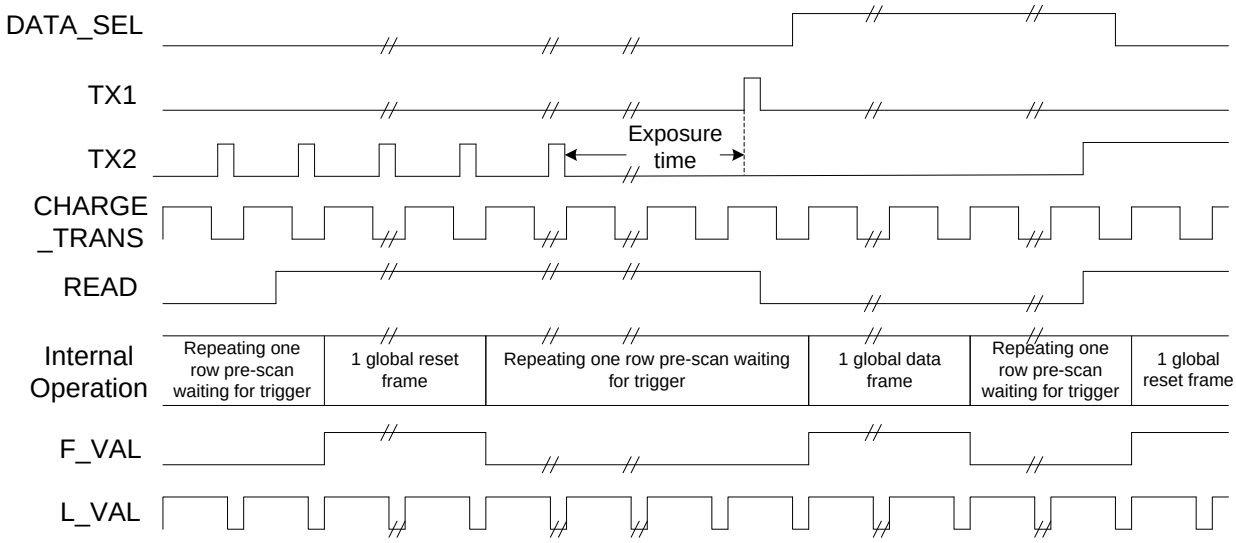


Figure 20. Global Shutter Mode with External Trigger

5.3 Region of Interest

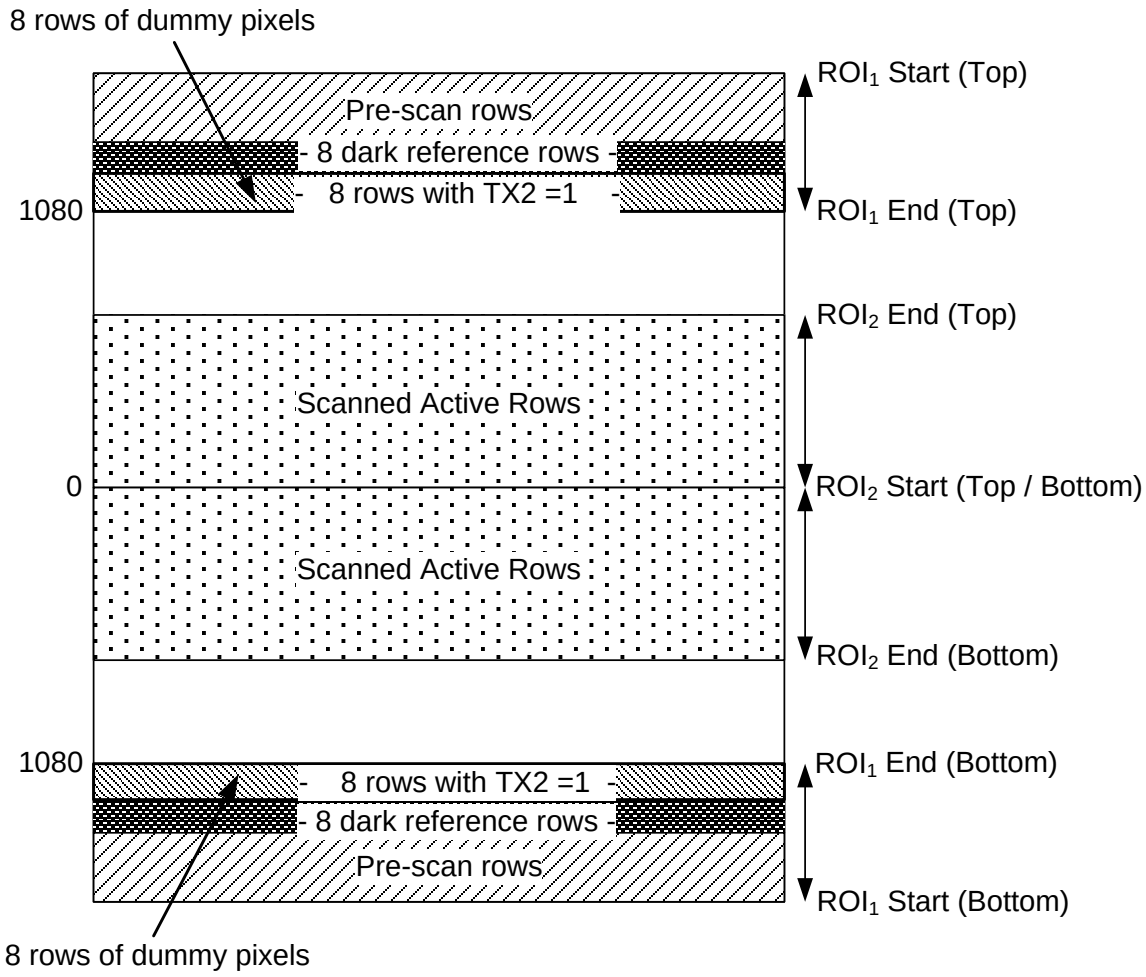


Figure 21. Programmable Regions of Interest

The row control supports two regions of interest (ROI). The first ROI defines the non-imaging region of interest: dark rows and pre-scan rows. It has a programmable size (JTAG Register 8) and a fixed end address of 1080 pointing to the start of the 8 dummy (also called “electrically dark”) rows, the pixels of which are optically shielded and have their TX2 gates tied to AVDD to dump all the charge out. The next 8 rows of the first ROI are dark reference rows where the pixels are covered by an opaque metal light shield. A size of 0 will suppress the output from this first ROI region. The direction of counting is always down, i.e. for a ROI_1 size greater than 0, counting will be from (1079 + size) down to 1080. If the row address is greater than 1095, no actual row is selected and the chip output data would correspond to background noise of the column circuits. This operation is termed “pre-scan”. For the pre-scan rows, the background noise level of the column amplifier circuits is equal to the floating diffusion node voltages of the last row of ROI2 to be read out. (When the number of pre-scan values is large, it is possible for dark current to build up on the floating diffusion nodes over the pre-scan readout period.) Pre-scan rows are also called virtual rows.

The second ROI is the region that contains all the light sensitive pixels. This region is called the active imager region. It has programmable start and end addresses. The counting direction of this ROI is computed automatically from the starting and ending addresses. If the ending address is greater than the starting address, the counting direction is from the center of the imager outward (i.e. up for the top half of the imager, down for the bottom half). Otherwise it is in the reverse direction (i.e. row counting proceeds toward the direction of the imager center). Figure 21 schematically shows the two ROIs in the top and bottom halves of the sensor.

Normally, a frame of data consists of the ROI1 rows preceding the ROI2 rows (pre-scan/dark/active imager). This order can be reversed if Register 2 bit 22 is set to 1 (not the default). In that case, a frame consists of the ROI2 rows followed by the ROI1 rows (active imager/pre-scan/dark).

L_VALID is asserted once each row readout, whether that row is pre-scan, dark, or active imager. F_VALID is asserted high once the first physical row of the frame is read out and goes low only after the last physical row of the frame is read out. Physical rows are dark rows and active imager rows. F_VALID will be low and stay low during the readout of pre-scan rows.

6 Electrical Specifications

6.1 DC Specifications

6.1.1 Power Inputs

Table 8: Power Input Parameters

Parameter	Pad Definition (Note 1)	Min	Typ	Max	Units
AVDD (Note 2)	Analog circuits power supply Ripple < 1mV RMS	3.135	3.3	3.465	V
I_{AVDD} (Note 2)	Analog circuits current		270, 355 (with 5% duty cycle)		mA
AVDD_PIX	Pixel source follower power supply Ripple < 100 µV RMS	3.135	3.3	3.465	V
I_{AVDD_PIX}	Pixel source follower current		25		mA
AVDD_RST1	Pixel reset power supply1 Ripple < 10 µV RMS	2.2	3.00	3.3	V
I_{AVDD_RST1}	Pixel reset 1 current		1		mA
AVDD_RST2 (Note 3)	Pixel reset power supply2 Ripple < 10 µV RMS	2.2	3.0 (Rolling Shutter) 2.739 (Global Shutter)	3.3	V
I_{AVDD_RST2}	Pixel reset 2 current		1		mA
DVDD_3V3	Row circuits and level shifters power supply Ripple < 1mV RMS	3.135	3.3	3.465	V
I_{DVDD_3V3}	Row circuit and level shifter current		1		mA
DVDD	Digital circuits power supply Ripple < 25 mV RMS	1.71	1.8	1.89	V
I_{DVDD}	Digital circuits current		290@287 MHz		mA
DVDD_IO (Note 4)	I/O circuits power supply Ripple < 25 mV RMS	1.71	1.8	1.89	V
I_{DVDD_IO} (Note 4)	I/O circuits current (with no terminations on outputs)		110@270 MHz		mA

Parameter	Pad Definition (Note 1)	Min	Typ	Max	Units
VTX1_POS	TX1 Transfer gate positive power supply Ripple < 1 mV RMS	2.90	3.3	3.60	V
I_{VTX1_POS}	TX1 Transfer gate positive current		1 (Rolling Shutter) 200 (Global Shutter 1µsec pulse)		mA
VTX1_NEG	TX1 Transfer gate negative supply Ripple < 100µV RMS	-1.5	-0.4	+0.3	V
I_{VTX1_NEG}	TX1 Transfer gate positive current		1 (Rolling Shutter) 200 (Global Shutter 1µsec pulse)		mA
VTX2_POS (Note 5)	TX2 Transfer gate positive power supply Ripple < 1 mV RMS	2.90	3.3	3.60	V
I_{VTX2_POS} (Note 5)	TX2 Transfer gate positive current		1 (Rolling Shutter) 200 (Global Shutter 1µsec pulse)		mA
VTX2_NEG (Note 6)	TX2 Transfer gate negative supply Ripple < 1 mV RMS	-1.5	-0.4 or +0.8	+0.85	V
I_{VTX2_NEG} (Note 6)	TX2 Transfer gate positive current		1 (Rolling Shutter) 200 (Global Shutter 1µsec pulse)		mA
$T_{operation}$	Sensor junction temperature	-40	30	+55	°C
RTRIM	Bias resistor for bandgap based internal bias generator (current through resistor is approximately 100µA; for low noise, place resistor close to sensor)	11K	12.28K (Note 7)	13.5K	Ω
PTAT R_{OUT}	Output resistance of PTAT temperature sensor (@ pin VPTAT)		100K (Note 8)		Ω

Note 1: Note that the power supplies with the tightest voltage ripple requirements are the ones closest to the pixel floating diffusion. RST1 and RST2 directly connect to the floating diffusion, so they have the tightest specs: less than 10 µV. VTX1_NEG and AVDD_PIX (which powers the Source Follower transistor on the pixel) are next at less than 100 µV ripple. VTX2_POS, VTX2_NEG, and VTX1_POS allow for the most (for voltages that touch the pixel) with a ripple voltage spec of less than 1 mV. (TX2 is further from the floating diffusion than TX1, and TX1 spends most of its time with VTX1_NEG on the TX1 gate, so that is the more critical of the TX1 voltages. The idea is to prevent power supply noise from capacitively coupling to the pixel floating diffusion.

Note 2: The relevant period for this duty cycle is the row readout time, which is 2624 SCLKs for both the default and recommended wavetables. The 5% number comes from the percentage of clock cycles that buff_en (wavetable bit 8) is high during the 2624 SCLK row readout time.

Note 3: The recommended voltage for AVDD_RST2 is 3.00 Volts when running in Rolling Shutter and 2.739 Volts when running in Global Shutter. If the user plans on switching between Rolling and Global Shutter, the power to AVDD_RST1 must be switchable between these two voltages. For Global Shutter operation, it is critical for there to be a tightly controlled differential between AVDD_RST1 and AVDD_RST2 – a 261 mV differential in the case of AVDD_RST1 = 3.000 V and AVDD_RST2 = 2.739 V. This is particularly critical for high gain Global Shutter operations. This differential voltage controls the DN level of the Reset frame, with a target of about 300 DN for the Reset frame being the goal. At 10x gain, each 10 mV of differential voltage changes the Reset level by 100 DN. At 30x gain, each 10 mV of differential voltage changes the Reset level by 300 DN.

Note 4: Normally the DOUT and DOUT_LG pins send their outputs to another chip (typically an FPGA) to be decoded from Gray code to binary. If the traces connecting the imager to this external chip are too long, the user may wish to add termination at the inputs to this other chip to prevent signal reflection. Adding such termination will increase the current requirement on DVDD_IO. (In practice, no BAE-designed cameras have required such termination.)

Note 5: In Rolling Shutter, the TX2 gate is not typically pulsed and the TX1 gate only gets pulsed for one row of pixels at a time. The current requirements of VTX1_POS, VTX2_POS, VTX1_NEG, and VTX2_NEG are therefore minimal (< 1 mA) in typical Rolling Shutter applications. In Global Shutter, both the TX1 and TX2 gates pulse globally (i.e. every pixel in the sensor pulsing simultaneously). In Global Shutter therefore, VTX1_POS, VTX2_POS, VTX1_NEG, and VTX2_NEG all must have enough current capacity to source or sink the necessary currents. For a Global TX2 pulse, the VTX2_POS must supply 200 mA on the rising edge of that pulse and the VTX2_NEG must sink 200 mA on the falling edge of that pulse. Similarly, for a Global TX1 pulse, the VTX1_POS must supply 200 mA on the rising edge of that pulse and the VTX1_NEG must sink 200 mA on the falling edge of that pulse. At a minimum, Global Shutter operation typically requires a single Global TX2 pulse and a single Global TX1 pulse. But sometimes (see Figures 17 and 22) there are Global TX2 pulse trains where these 200 mA source/sink current requirements are needed each line time. The 200 mA number is for the imager as a whole. The number for each imager half is 100 mA.

Note 6: The recommended voltage for VTX2_NEG is -0.4 Volts when running in Global Shutter.

-0.4 Volts is also recommended when running in Rolling Shutter under low light conditions. But when running in Rolling Shutter under high light conditions, +0.8 Volts is recommended. This voltage setting will make use of the TX2 gate's anti-blooming functionality

Note 7: There are two RTRIM pins on the packaged part, pins 75 and 96. For each pin, a 12.28 KΩ resistor should be attached with one end to the RTRIM pin and with the other end at analog ground. These two resistors are important in order to power the column amplifier circuits and insure functioning DOUT and DOUT_LG outputs.

Note 8: The 100KΩ resistance is an internal resistance inside the chip. The user does not need to add any external resistor. The 100KΩ number is given so that when the user measures the PTAT voltage, the user will choose a voltmeter with an internal impedance much greater than 100KΩ so as not to load the PTAT pin and get an inaccurate voltage reading. PTAT stands for Proportional To Absolute Temperature.

6.1.2 Power Consumption

Table 9: Power Consumption (Active and Standby Modes)

Parameter	Nominal	Maximum	Units
Total power consumption	0.7 (Low gain only 50 fps) 1.5 (Dual channel 100fps)		Watts

6.1.3 HSTL I/O DC Specifications

Table 10: HSTL DC Specifications

Symbol	Parameter	Min	Nom	Max	Conditions
V_{REF}	HSTL reference voltage	0.855	0.9	0.945	0.5*DVDD
V_{TT}	HSTL termination voltage	0.855	0.9	0.945	0.5*DVDD
$V_{IH(dc)}$	DC input logic high	V_{REF} + 0.1		DVDD + 0.3	V
$V_{IL(dc)}$	DC input logic low	-0.3		V_{REF} - 0.1	V
$V_{OH(dc)}$	DC output logic high	DVDD - 0.5			V
$V_{OL(dc)}$	DC output logic low			0.5	V
$I_{OH(dc)}$	Output minimum source DC current	-10 mA			@ $V_{OH(dc)}$= DVDD - 0.5
$I_{OL(dc)}$	Output minimum sink DC current	10 mA			@ $V_{OL(dc)}$= 0.5

6.1.4 LVCMOS I/O DC Specifications

Table 11: LVCMOS DC Specifications

Symbol	Parameter	Min	Nom	Max	Conditions
$V_{IH(dc)}$	DC input logic high	0.7*DVDD		DVDD + 0.3	V
$V_{IL(dc)}$	DC input logic low	-0.3		0.3*DVDD	V

6.1.5 Power Up/Down Sequence

Fairchild Imaging recommends that the power up sequence follows the order shown below:

1. First, DVDD and DVDD_IO should be powered-up with all the analog supplies held low, with DVDD_3V3 held low, and with both RESETB and READ held low.
2. Next, SCLK should be activated (SCLK_TP and SCLK_BT if running both halves) for a minimum of 8 cycles before proceeding.
3. Then, the sensor should be taken out of reset with both RESETB and READ going high. If both sensor halves are to be frame-synchronized, the READ_TP and READ_BT signal edges have to be applied simultaneously. SCLK should be clocked for at least one frame time before proceeding to next step.
4. At this point, taking the sensor back into reset is optional. (For example, setting the READ pin to 0 at this point would make it possible to program the registers with non-default values. When this task is done, READ should be set high again.)
5. Now, AVDD and all other analog power supplies can be brought up. DVDD_3V3 is also to be brought up at this time.

6.1.6 Power down sequence

All the power supplies can be brought down simultaneously.

6.1.7 Selective component power down

A JTAG register (Register 3) is provided to selectively power down individual circuits in order to reduce noise and power dissipation of the sensor under some modes of operation. This register is activated by setting JTAG Register 2 (mode register) bit 25 (low power activation) to 1.

6.2 AC Specifications

6.2.1 Input Capacitance

Table 12: Input Capacitance

I/O Type	Parameter	Typical	Unit
INPUT (digital)	Cind	5	pF
INPUT (power)	Cinp	< 1	nF

6.3 Timing

6.3.1 JTAG Timing

JTAG timing is shown in Figure 22 and Table 13.

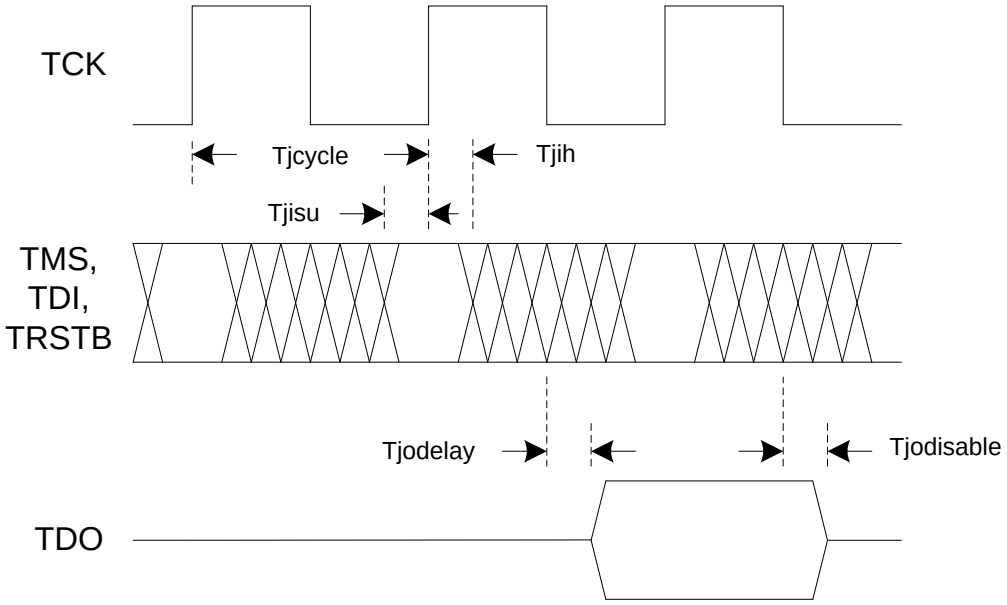


Figure 22. JTAG Interface I/O Timing

Table 13: Timing Parameter Definitions for JTAG Interface I/O Timing

Parameter	Definition	Unit	Min	Max	Note
Tjcycle	TCK clock cycle time	ns	40		
Tjdc	TCK clock duty cycle	%	45	55	
Tjisu	TMS, TDI, TRSTB input setup time	ns	2.0		
Tjih	TMS, TDI, TRSTB input hold time	ns	1.0		
Tjodelay	TDO output delay time from falling edge of TCK	ns		8.0	
Tjodisable	TDO output disable time from falling edge of TCK	ns		6.0	

6.3.2 Functional Control Input Timing

Functional control input timing is shown in Figure 23 and Table 14.

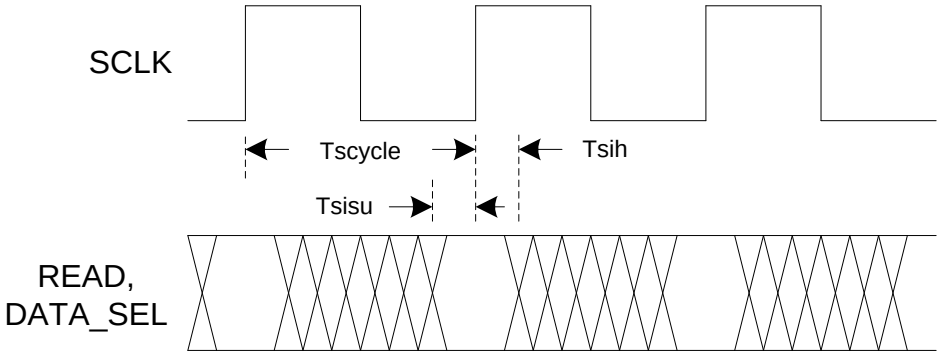


Figure 23. Functional Control Inputs Timing

Table 14: Functional Control Inputs Timing

Parameter	Definition	Unit	Min	Max	Note
Tscycle	SCLK clock cycle time	ns	3.53		
Tsdc	SCLK clock duty cycle	%	48	52	
Tsjitter	SCLK peak to peak cycle jitter	ps		150	
Tsisu	READ, DATA_SEL input setup time	ns	1.0		
Tsih	READ, DATA_SEL input hold time	ns	0.5		

6.3.3 Data and Status Output Timing

Timing for data and status outputs are shown in Figure 24 and Table 15.

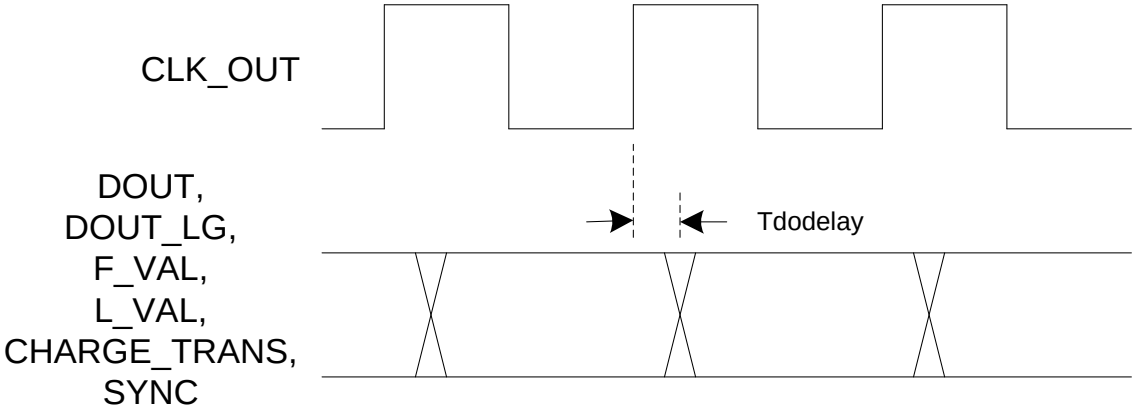


Figure 24. Data and Status Output Timing

Table 15: Data and Status Output Timing

Parameter	Definition	Unit	Min	Max	Note
Tdodelay	DOUT, DOUT_LG, F_VALID, L_VALID CHARGE_TRANS, SYNC output delay time	ns		1.5	Source Synchronous

7 Thermal, Mechanical and Part Ordering Information

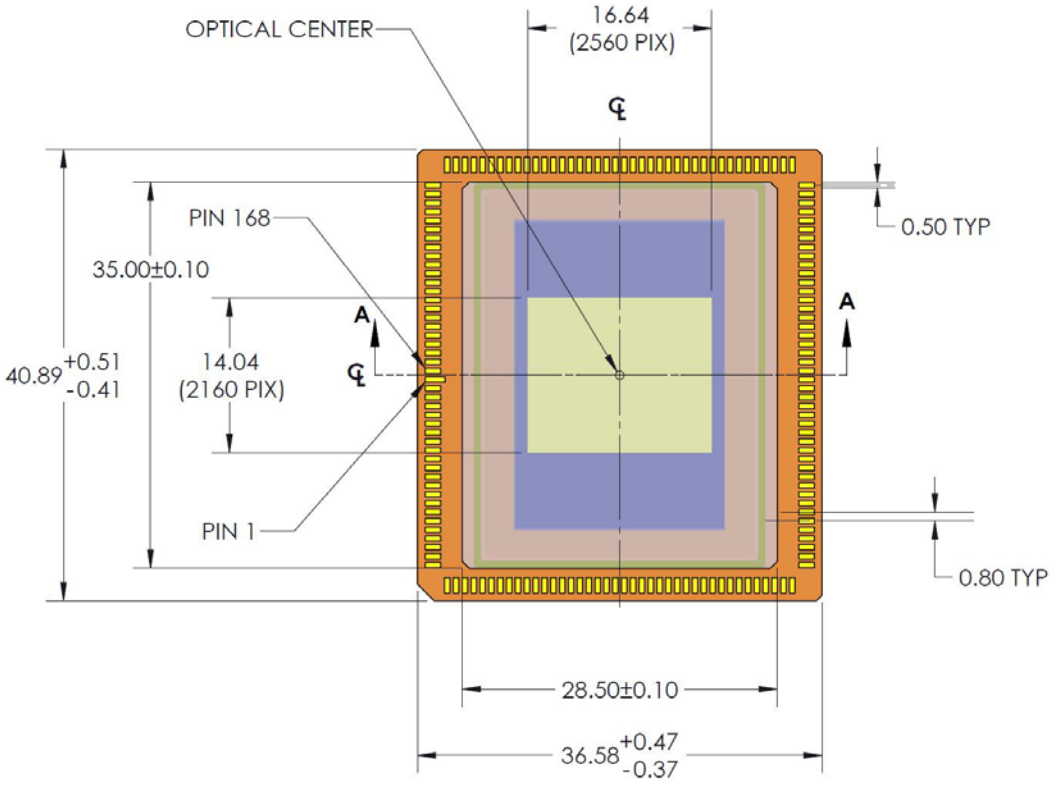
7.1 Thermal Specifications

Table 16: Thermal Specifications

Parameter	Minimum	Maximum	Units
$T_{operation}$ (Sensor junction temperature)	-40	+55	ºC
Storage temperature range	-40	+85	ºC

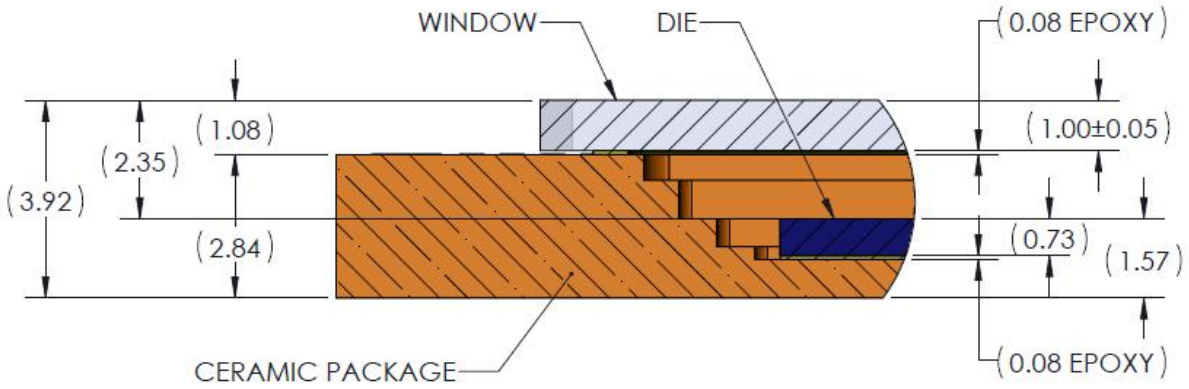
7.2 Package drawings

7.2.1 FX1 Scientific Package drawings



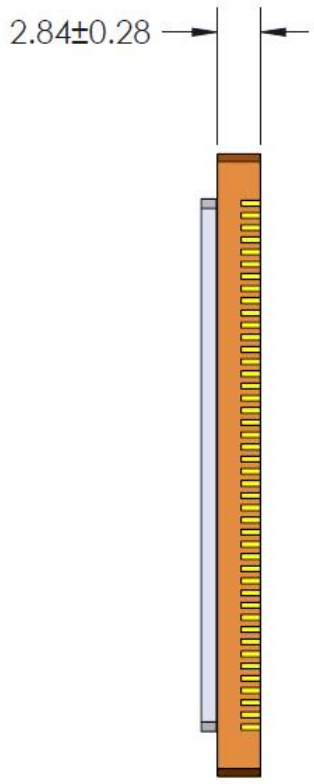
All dimensions are in mm.

Figure 25. Top View for CIS2521AF FX1 Scientific Package



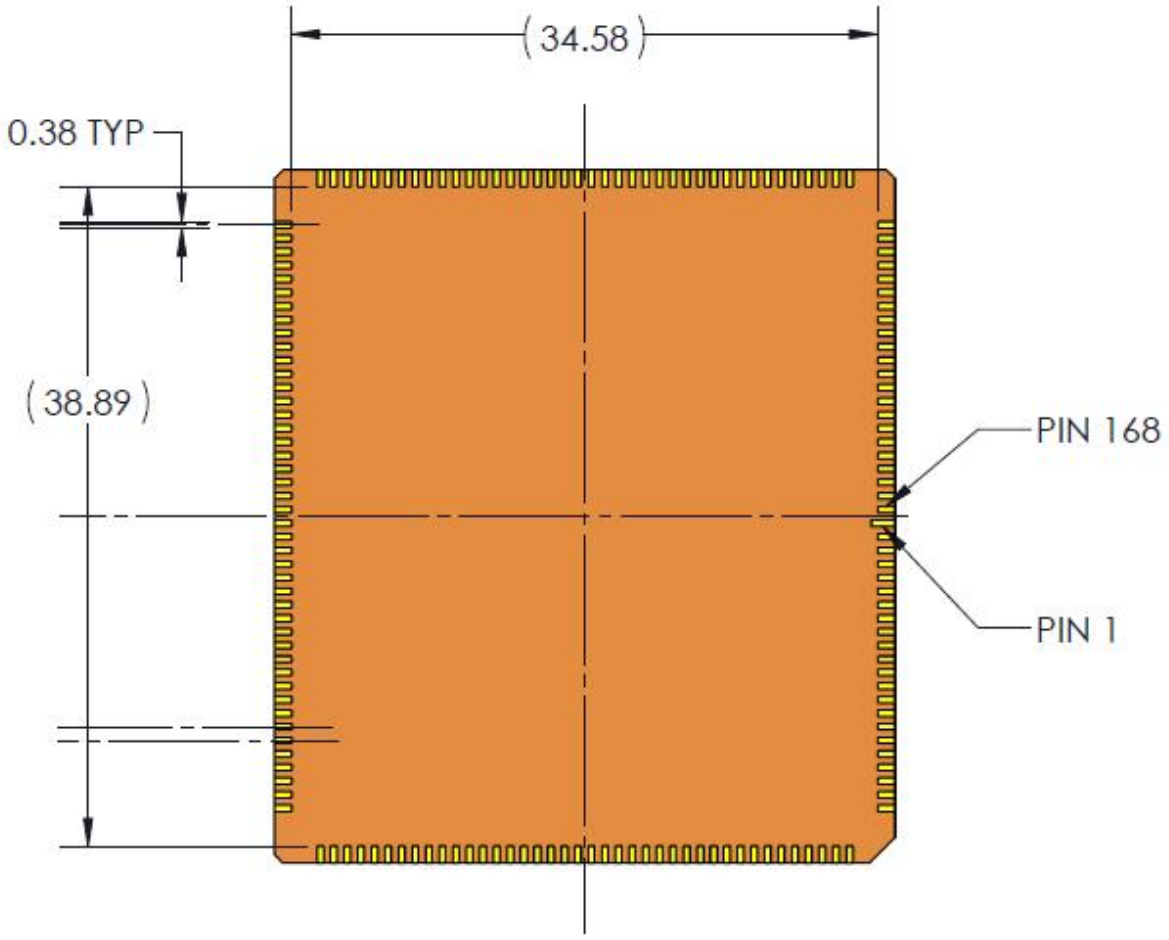
All dimensions are in mm.

Figure 26. Cross section View of CIS2521AF FX1 Scientific Package



All dimensions are in mm.

Figure 27. Side View of CIS2521AF FX1 Scientific Package

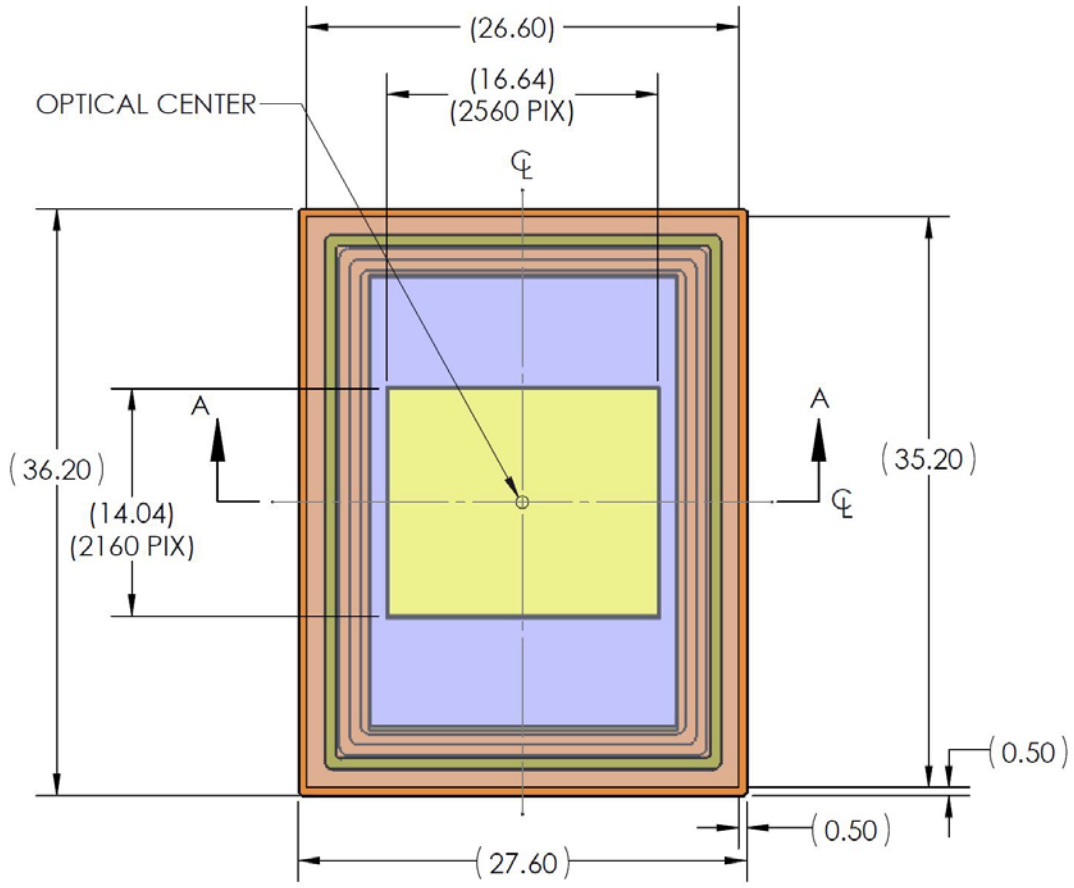


All dimensions are in mm.

Figure 28. Bottom View of CIS2521AF FX1 Scientific Package

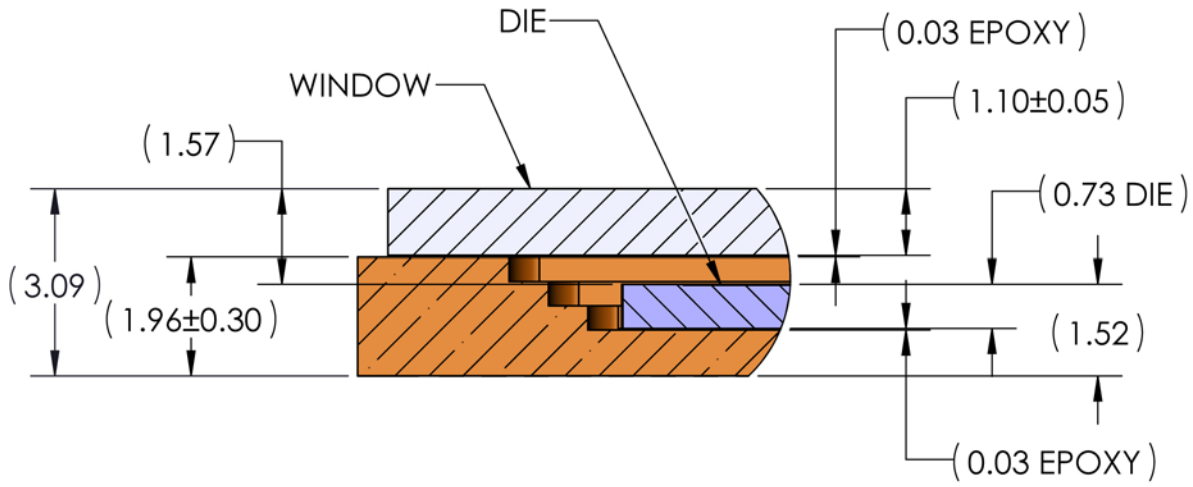
The scientific package has a die placement spec (corners of die to package corner fiducials) of +/- 2.5 mils. The die rotation spec (relative to the package sides) is < 125 microns. The die tilt spec (relative to the package bottom) is < 125 microns.

7.2.2 FX2 Standard Package Drawings



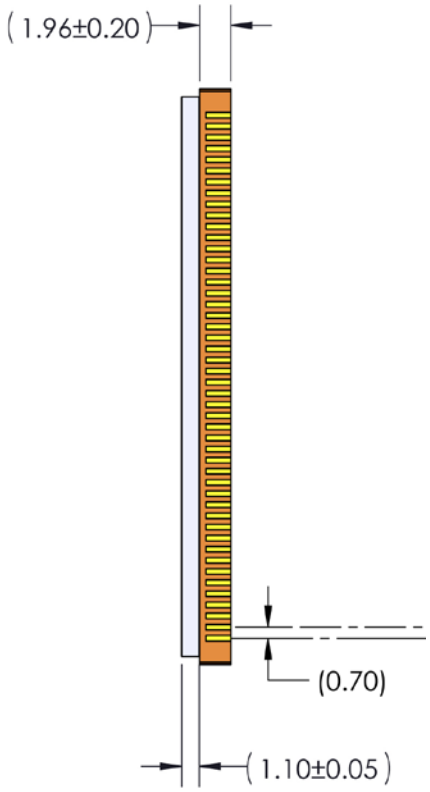
All dimensions are in mm.

Figure 29. Top View of CIS2521AF FX2 Standard Package



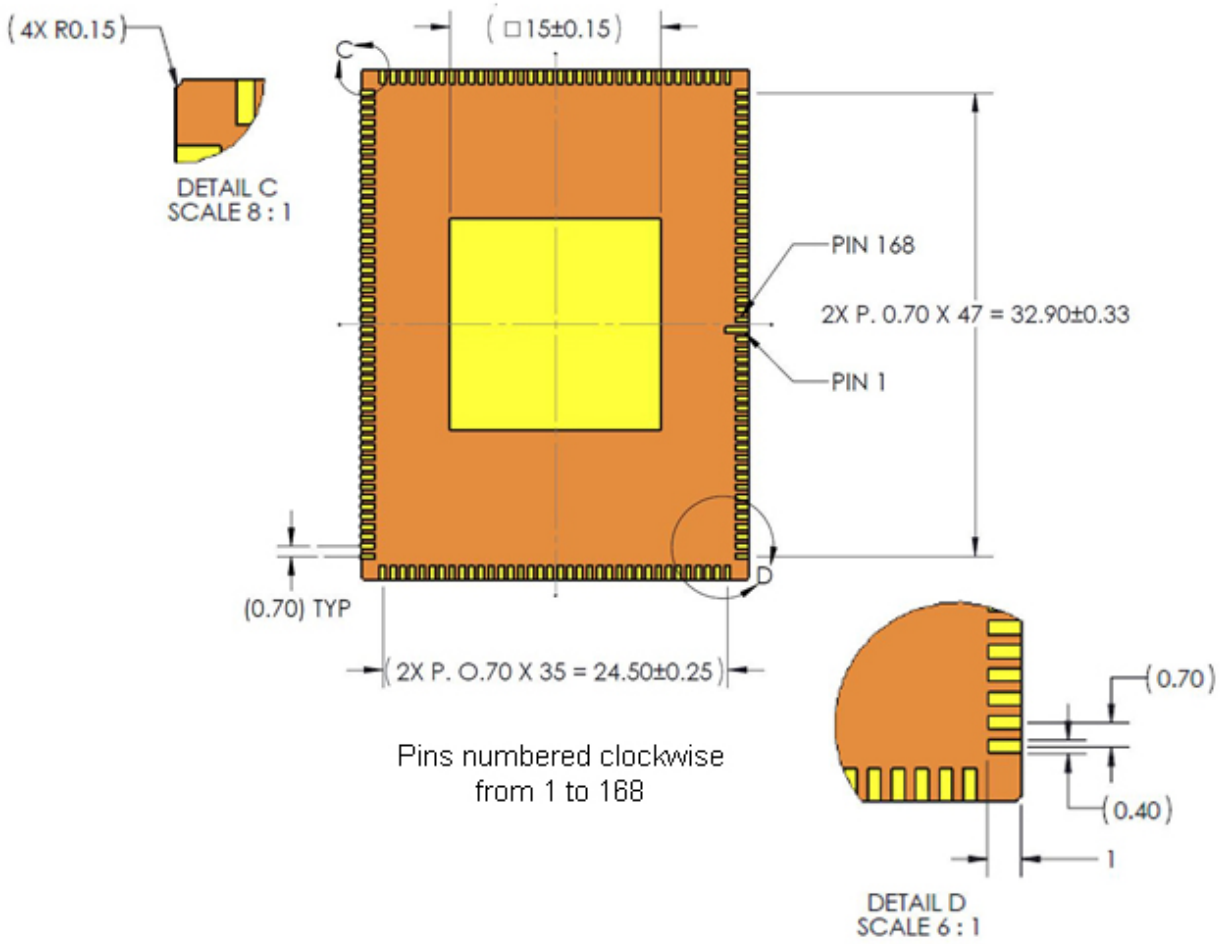
All dimensions are in millimeters.

Figure 30. Cross Section View of CIS2521AF FX2 Standard package



All dimensions are in millimeters.

Figure 31. Side View of CIS2521AF FX2 Standard Package



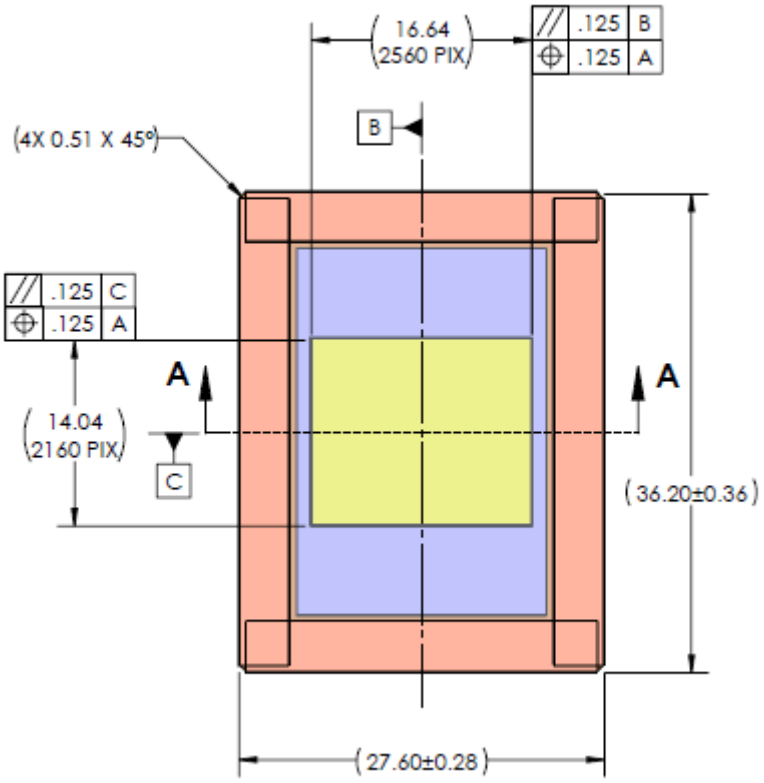
All dimensions are in millimeters.

Figure 32. Bottom View of CIS2521AF FX2 Standard Package

The standard package has a die placement spec (optical center of die to package center) of +/- 4 mils. The die rotation spec (relative to the package sides) is < 1°. The die tilt spec (relative to the package bottom) is < 1°.

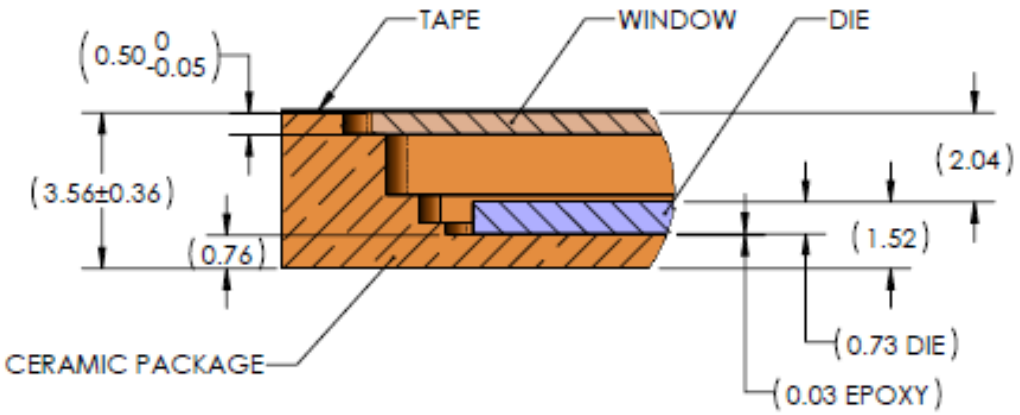
The thermal pad at the bottom of the package should be grounded.

7.2.3 FX4 Standard Package Drawings



All dimensions are in mm. FX4 package is shown with Temporary window.

Figure 33. Top View of CIS2521AF FX4 Standard Package

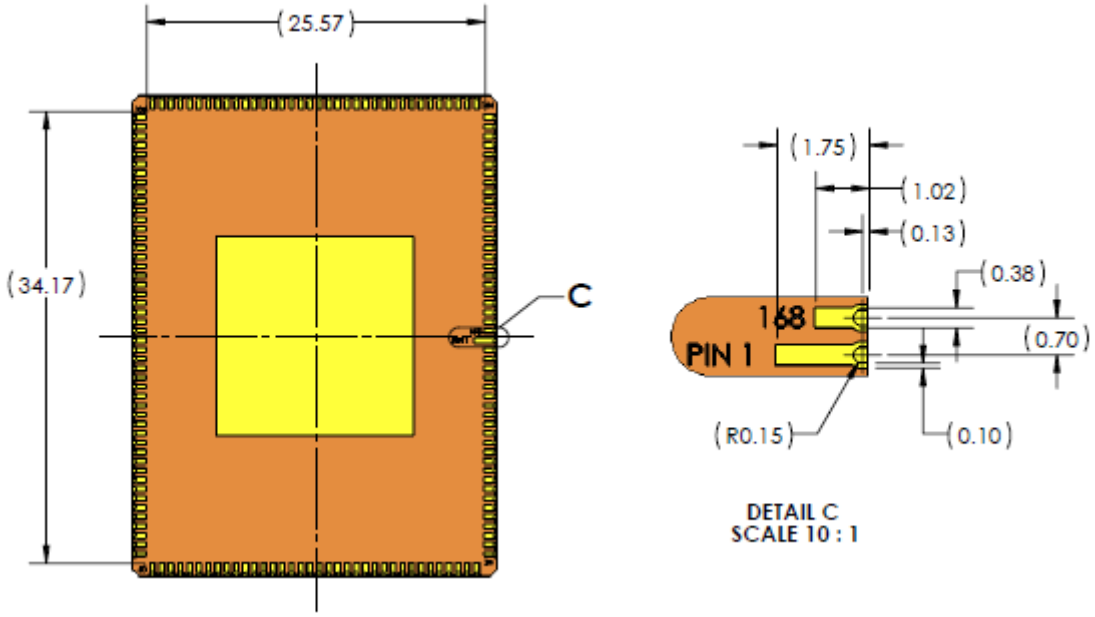


All dimensions are in millimeters. FX4 package is shown with Temporary window.

Figure 34. Cross Section View of CIS2521AF FX4 Standard package

All dimensions are in millimeters. FX4 package is shown with Temporary window.

Figure 35. Side View of CIS2521AF FX4 Standard Package



All dimensions are in millimeters.

Figure 36. Bottom View of CIS2521AF FX4 Standard Package

Pins are numbered 1 to 168 with Pin 1 being the larger pin. When viewed from the bottom, Pin 1 is on the right side (in the middle). Pins increment in number moving clockwise around the part until Pin 168 is reached.

The FX4 standard package has a die placement spec (optical center of die to package center) of +/- 4 mils. The die rotation spec (relative to the package sides) is < 1°. The die tilt spec (relative to the package bottom) is < 1°.

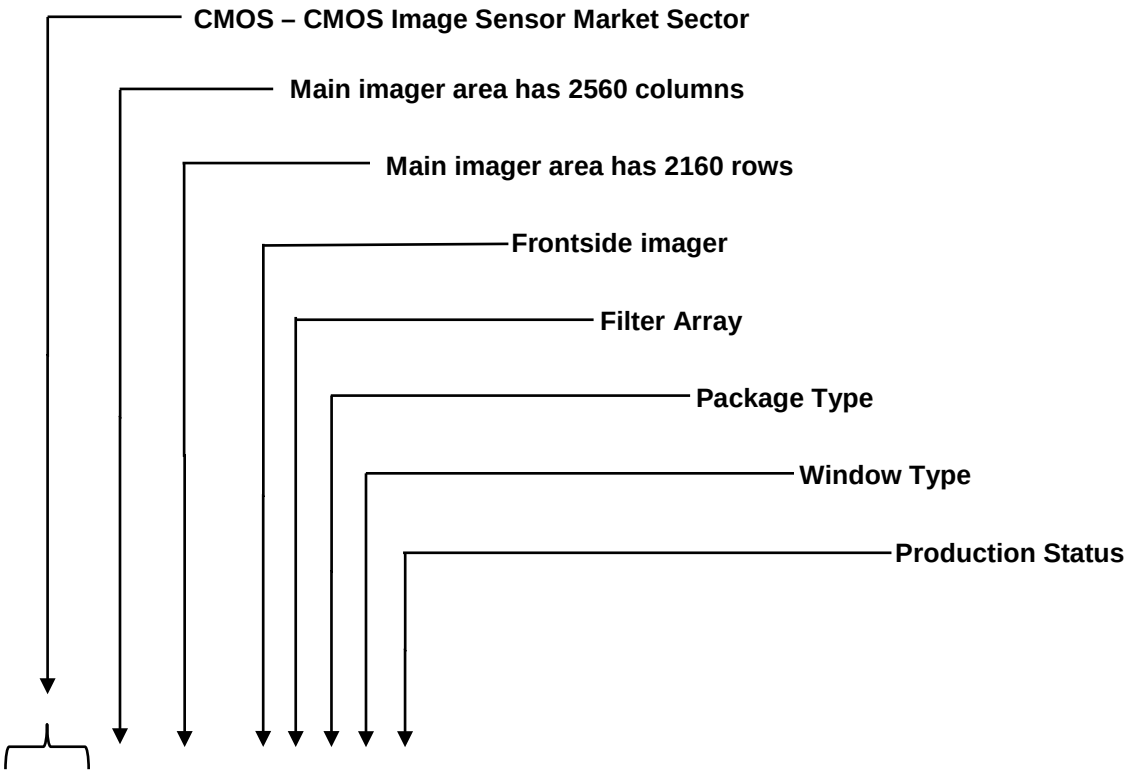
The thermal pad at the bottom of the package should be grounded.

7.3 Part Numbering

Table 17. Ordering Part Number

Part Number	Description
CIS2521AF0111	Monochrome, FX1 Scientific package, Temporary window
CIS2521AF0121	Monochrome, FX1 Scientific package, Sealed window
CIS2521AF0211	Monochrome, FX2 Standard package, Temporary window
CIS2521AF0221	Monochrome, FX2 Standard package, Sealed window
CIS2521AF0411	Monochrome, FX4 Standard package, Temporary window
CIS2521AF1111	Color, FX1 Scientific package, Temporary window
CIS2521AF1121	Color, FX1 Scientific package, Sealed window
CIS2521AF1221, CIS2521AF1222	Color, FX2 Standard package, Sealed window
CIS2521AF1411	Color, FX4 Standard package, Temporary window

Part Numbering Decoder



Filter Array (FA)

1 = Bayer RGB color
0 = Monochrome

Package Type

4 = FX4 Standard
2 = FX2 Standard
1 = FX1 Scientific

Window Type

2 = Sealed Window with Anti-Reflection coating on both sides
1 = Temporary Window

Production Status

1 = Production Release
2 = Production Release with Custom marking

8 Monochromatic Quantum Efficiency

Unless otherwise specified, this datasheet assumes the CIS2521AF sensor is monochromatic (i.e. it has no color filter), and a typical monochromatic QE curve is shown in Figure 37. However, adding a color filter is an option with the CIS2521AF. The color filter spatial arrangement is shown in Figure 38 and the QE curves of the RGB color filters are shown in Figure 39.

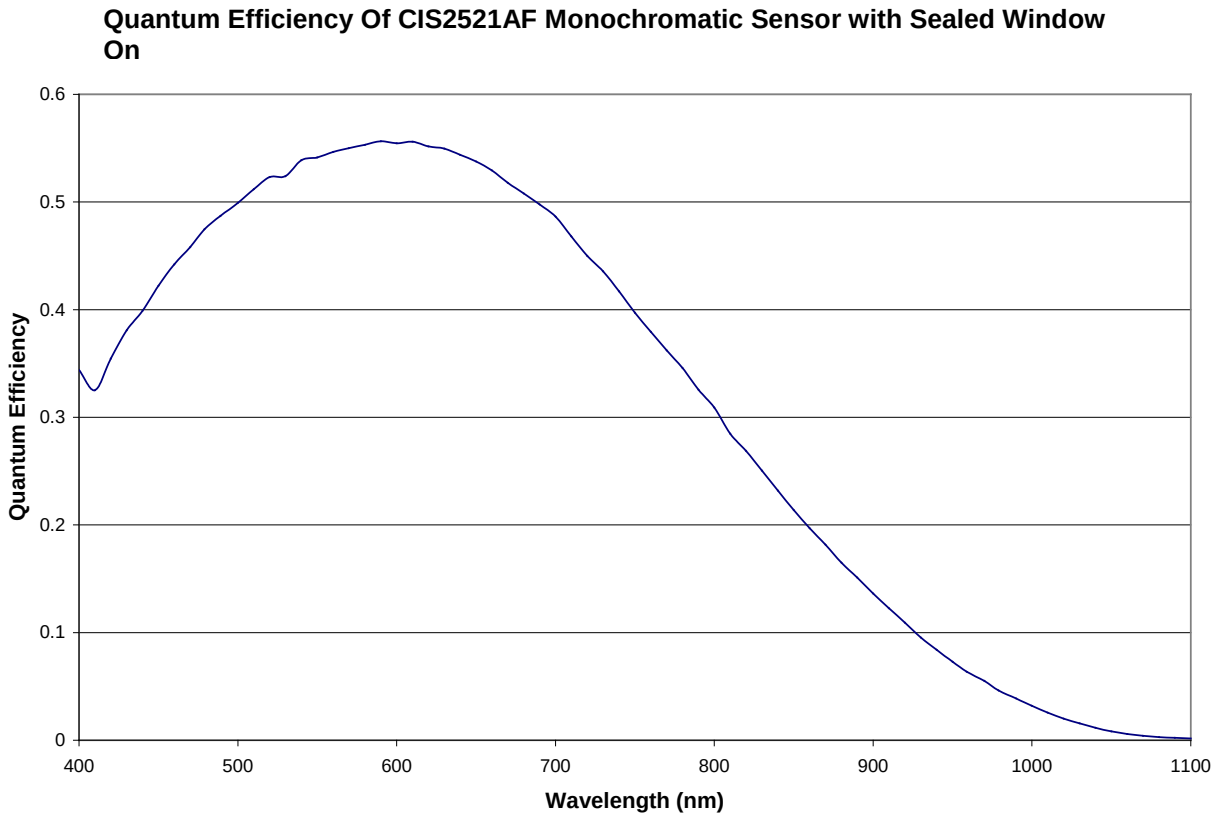


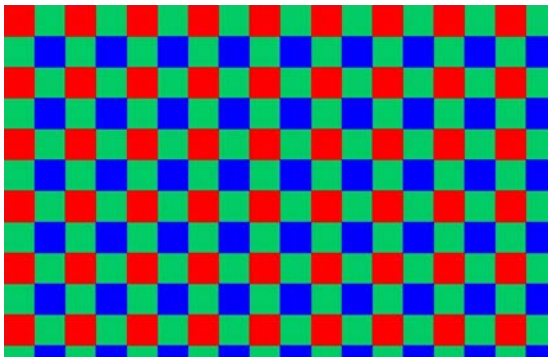
Figure 37. Quantum Efficiency of Monochromatic CIS2521AF

A table showing the monochromatic Quantum Efficiency at increments of 10 nm is shown on the next page. Values shown are typical. Data was taken with the sealed window on.

Table 18: Monochromatic Quantum Efficiency vs. Wavelength

WaveLength	Monochromatic	WaveLength	Monochromatic	WaveLength	Monochromatic
400 nm	0.34	640 nm	0.54	880 nm	0.17
410 nm	0.33	650 nm	0.54	890 nm	0.15
420 nm	0.35	660 nm	0.53	900 nm	0.14
430 nm	0.38	670 nm	0.52	910 nm	0.12
440 nm	0.40	680 nm	0.51	920 nm	0.11
450 nm	0.42	690 nm	0.50	930 nm	0.10
460 nm	0.44	700 nm	0.49	940 nm	0.08
470 nm	0.46	710 nm	0.47	950 nm	0.07
480 nm	0.47	720 nm	0.45	960 nm	0.06
490 nm	0.49	730 nm	0.44	970 nm	0.06
500 nm	0.50	740 nm	0.42	980 nm	0.05
510 nm	0.51	750 nm	0.40	990 nm	0.04
520 nm	0.52	760 nm	0.38	1000 nm	0.03
530 nm	0.52	770 nm	0.36	1010 nm	0.03
540 nm	0.54	780 nm	0.35	1020 nm	0.02
550 nm	0.54	790 nm	0.33	1030 nm	0.02
560 nm	0.55	800 nm	0.31	1040 nm	0.01
570 nm	0.55	810 nm	0.28	1050 nm	0.01
580 nm	0.55	820 nm	0.27	1060 nm	0.01
590 nm	0.56	830 nm	0.25	1070 nm	0.00
600 nm	0.55	840 nm	0.23	1080 nm	0.00
610 nm	0.56	850 nm	0.21	1090 nm	0.00
620 nm	0.55	860 nm	0.20	1100 nm	0.00
630 nm	0.55	870 nm	0.18		

9 Color Filter Array (CFA) Option and Color QE



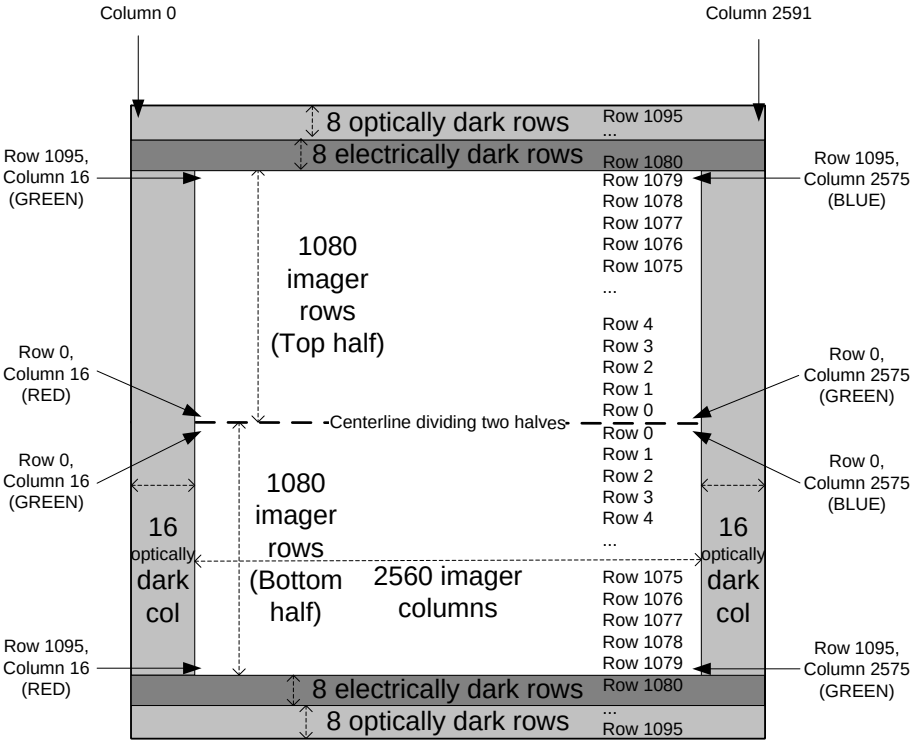


Figure 38. Color Filter Array

The Bayer pattern RGB Color Filter Array (CFA) covers the 2560 (H) x 2160 (V) imaging pixels and extends 2 pixels deep into the dark pixels region on all 4 sides.

For the top half of the sensor, even numbered rows are Red/Green, with even columns Red and odd columns Green. Odd numbered rows are Green/Blue, with even columns Green and odd columns Blue.

For the bottom half of the sensor, even numbered rows are Green/Blue, with even columns Green and odd columns Blue. Odd numbered rows are Red/Green, with even columns Red and odd columns Green.

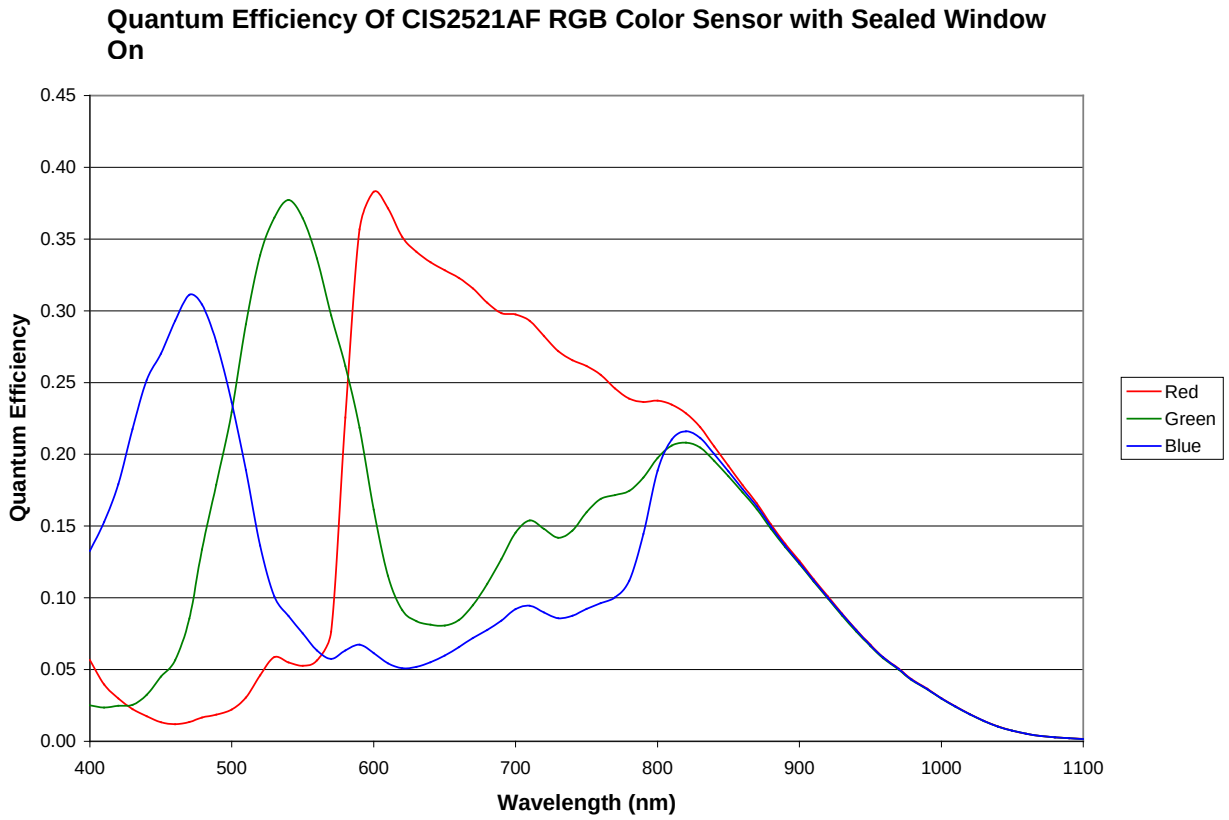


Figure 39. CFA QE Curves

A table showing the RGB color Quantum Efficiency at increments of 10 nm is shown on the next page. Values shown are typical. Data was taken with the sealed window on.

Table 19: RBG Color Quantum Efficiency vs. Wavelength

WaveLength	Red	Green	Blue	WaveLength	Red	Green	Blue
400 nm	0.06	0.03	0.13	760 nm	0.26	0.17	0.10
410 nm	0.04	0.02	0.15	770 nm	0.25	0.17	0.10
420 nm	0.03	0.02	0.18	780 nm	0.24	0.17	0.11
430 nm	0.02	0.03	0.22	790 nm	0.24	0.18	0.14
440 nm	0.02	0.03	0.25	800 nm	0.24	0.20	0.19
450 nm	0.01	0.05	0.27	810 nm	0.23	0.21	0.21
460 nm	0.01	0.06	0.29	820 nm	0.23	0.21	0.22
470 nm	0.01	0.09	0.31	830 nm	0.22	0.20	0.21
480 nm	0.02	0.13	0.30	840 nm	0.21	0.20	0.20
490 nm	0.02	0.18	0.28	850 nm	0.19	0.18	0.19
500 nm	0.02	0.23	0.24	860 nm	0.18	0.17	0.18
510 nm	0.03	0.29	0.19	870 nm	0.17	0.16	0.16
520 nm	0.05	0.34	0.14	880 nm	0.15	0.15	0.15
530 nm	0.06	0.36	0.10	890 nm	0.14	0.14	0.14
540 nm	0.05	0.38	0.09	900 nm	0.13	0.12	0.12
550 nm	0.05	0.36	0.08	910 nm	0.11	0.11	0.11
560 nm	0.06	0.34	0.06	920 nm	0.10	0.10	0.10
570 nm	0.08	0.30	0.06	930 nm	0.09	0.09	0.09
580 nm	0.23	0.26	0.06	940 nm	0.08	0.08	0.08
590 nm	0.36	0.22	0.07	950 nm	0.07	0.07	0.07
600 nm	0.38	0.16	0.06	960 nm	0.06	0.06	0.06
610 nm	0.37	0.12	0.05	970 nm	0.05	0.05	0.05
620 nm	0.35	0.09	0.05	980 nm	0.04	0.04	0.04
630 nm	0.34	0.08	0.05	990 nm	0.04	0.04	0.04
640 nm	0.33	0.08	0.06	1000 nm	0.03	0.03	0.03
650 nm	0.33	0.08	0.06	1010 nm	0.02	0.02	0.02
660 nm	0.32	0.08	0.07	1020 nm	0.02	0.02	0.02

WaveLength	Red	Green	Blue	WaveLength	Red	Green	Blue
670 nm	0.32	0.09	0.07	1030 nm	0.01	0.01	0.01
680 nm	0.31	0.11	0.08	1040 nm	0.01	0.01	0.01
690 nm	0.30	0.13	0.08	1050 nm	0.01	0.01	0.01
700 nm	0.30	0.15	0.09	1060 nm	0.01	0.01	0.01
710 nm	0.29	0.15	0.09	1070 nm	0.00	0.00	0.00
720 nm	0.28	0.15	0.09	1080 nm	0.00	0.00	0.00
730 nm	0.27	0.14	0.09	1090 nm	0.00	0.00	0.00
740 nm	0.27	0.15	0.09	1100 nm	0.00	0.00	0.00
750 nm	0.26	0.16	0.09				

10 Cosmetic Specifications

Table 20: Cosmetic Defect Classifications / Criteria / Counts

Defect classification	Criteria	Maximum Count	Comments
Hot Pixels in Dark Frame	± 6 sigma from the mean	4000	Low gain only
Cold/Warm Pixels in Light Frame – Minor Defects	> 15% from the mean	4000	Low gain only
Cold/Warm Pixels in Light Frame – Major Defects	> 50% from the mean	50	Low gain only
Small Cluster in Light Frame – Qty Allowed	± 6 sigma from the mean 2 < Size <= 20pix	50	Low gain only
Large Cluster in Light Frame– Qty Allowed	± 6 sigma from the mean Size > 20pix	0	Low gain only
Column -- Qty Allowed	± 10% gain variation from the mean	0	Low gain only
Row -- Qty Allowed	± 10% gain variation from the mean	0	Low gain only
Blob on Sealed Window	Must not be visible under illumination with camera lens at F#9 (or smaller F#)	0	Blob is defined as 50 contiguous pixels for mono sensor, 25 contiguous pixels in green pixel truncated image for color sensor

10.1 Test conditions

Blemish tests are performed in Rolling Shutter mode at 80 MHz; light frame captured at 50% of saturation.

Blemish specification applies to ROI: Center 2040 (H) x 2032 (V).

11 Handling Precautions

11.1 ESD Protection

To avoid damaging the device during handling, special care must be used with strict ESD controls. Use only ESD protected tools and ESD protected workstations. Operators must be equipped with approved ESD safe garments and use approved grounding equipment.

11.2 Moisture Protection

The Moisture Sensitivity Level (MSL) of the package is MSL 2, which means the package can resist moisture ingress under conditions of 30°C and 60% relative humidity for a year or more.

11.3 Soldering Requirements

For soldering the part, the temperature should not exceed 245°C for more than 60 seconds. Follow temperature ramp guidelines in JEDEC/IPC standard J-STD-020, current revision, for the IR/Convection oven reflow profile.

The taped on temporary windows of both the FX1 Scientific package and FX4 Standard package can be run through the reflow oven with the tape and the taped on temporary window in place.

11.4 Cleaning Requirements

For cleaning the window, first recognize the active area of the sensor. The active area of the sensor is the gray/silver area, which is surrounded by the inactive blue area. Only the window surface above the active area needs to be cleaned. Do not pour solvent or any liquid directly on to the window surface. Use a clean, lint-free swab. Dip the swab in methanol or isopropyl alcohol and carefully wipe the surface of the window. Clean, dry air can also be used to blow particle contamination off the window.

Cleaning the sensor active area surface itself is not recommended.

For cleaning the sensor package, use a clean, lint-free swab, dipping the swab in methanol or isopropyl alcohol and carefully wiping the sensor package. Acetone can also be used to clean the sensor package, but only if it can be kept away from the window seal epoxy. Clean, dry air can also be used to blow particle contamination off the window.

12 Revision History

Table 21: Revision History

Date	Revision	Description
June 2011	NR	Initial Release
July 2011	A	Incorporated Recommended Settings
March 2012	B	Deleted references to DOUT pins multiplexing, clarified DVDD_3V3 power on, added sealed window die stack up figure
August 2012	C	Added soldering and cleaning instructions. Added figure with row numbering. Extended pin descriptions and explanatory notes. Included Standard package drawing and updated Scientific package drawings. Changed sensor name from CIS2051 to CIS2521
December 2012	D	Added die placement, tilt and rotation specs. Clarified standard package thermal pad grounding. Changed sensor nomenclature to have 4 digit suffix. Added revision disclaimer.
February 2013	E	Changed Standard Package drawings, fixed typos, clarified TX1 and TX2 current requirements for Global Shutter pulses. Added Standard package photo to front page. Added HSTL class number. Added optical format. Increased maximum soldering temperature to 245°C.
October 2013	F	Tightened Lag spec, added debris (“blob”) spec for sealed window glass, corrected external trigger READ sampling point.
May 2014	G	Complete restructuring of document. Updated sequence of sections. Combined power and ground pads in Table 4. Combined signals in Table 6. Combined voltage and currents specs in Table 8. Added Figure 8. Signal Groups. Added Section 11 Handling Precautions. Updated package drawings for Package drawings.
June 2014	H	Found 20 references to CIS2521 and changed them to CIS2521F. Made datasheet consistent.
June 2016	J	Added FX4 package. Updated available product list.
January 2018	K	Changed part name from CIS2521F to CIS2521AF.

13 Disclaimer

BAE Systems reserves the right to make any changes to this product during an existing contract period providing it does not materially affect the form, fit or function of a Customer's next assembly product with BAE Systems' previously released design.

14 Contact Information

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